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**MS-7B19** mATX  
Ver: 11

## Coffeelake Platform

**CPU:** Coffeelake S

**PCH:** B360

**SPI ROM : 128 MB**

**Memory:** DDR4 \* 4 (Dual Channel)

**Power Solution:**

**CPU :** RT3607

**VCCSA :** NB685

**VCCIO :** SY8288

**DDR :** RT8231

**PCH :** RT8125E

**ACPI:** MPS

**Onboard Chip:**

**LAN** RTL8111H

**Dual Codec:** ALC887

**SIO:** NTC6797

**Type C:** ASM1543

**USB3 Redrive :** ASM1464 X 1

**Expansion Slots:**

**PCI Express (X16) Slot \* 1**

**PCI Express (X1 ) Slot \* 2**

**M.2 Slot (Socket 1 ) \* 1**

**LED**

**EZ Debug LED**

**Audio Line LED**

**Rear I/O Connectors**

**PS2**

**USB2.0x2**

**USB3.1 Gen1x4**

**RJ45 + USB3.1 (Type C+ A)**

**Audio Jack 3 Port**

**HDMI+DVI+VGA)**

**Internal Connectors**

**Dual SATA \* 3**

**FUSB3.0 Header \* 1**

**FUSB2.0 Header \* 2**

**Front Audio Header \* 1**

**Front Panel Header \* 2**

**SPI Header \* 1**

**TPM Header \* 1**

**CPU Fan \* 1**

**System Fan \* 2**

**Internal Pin Header**

**JRGB1**

**JSPI1**

**JCI1**

**JBAT1**

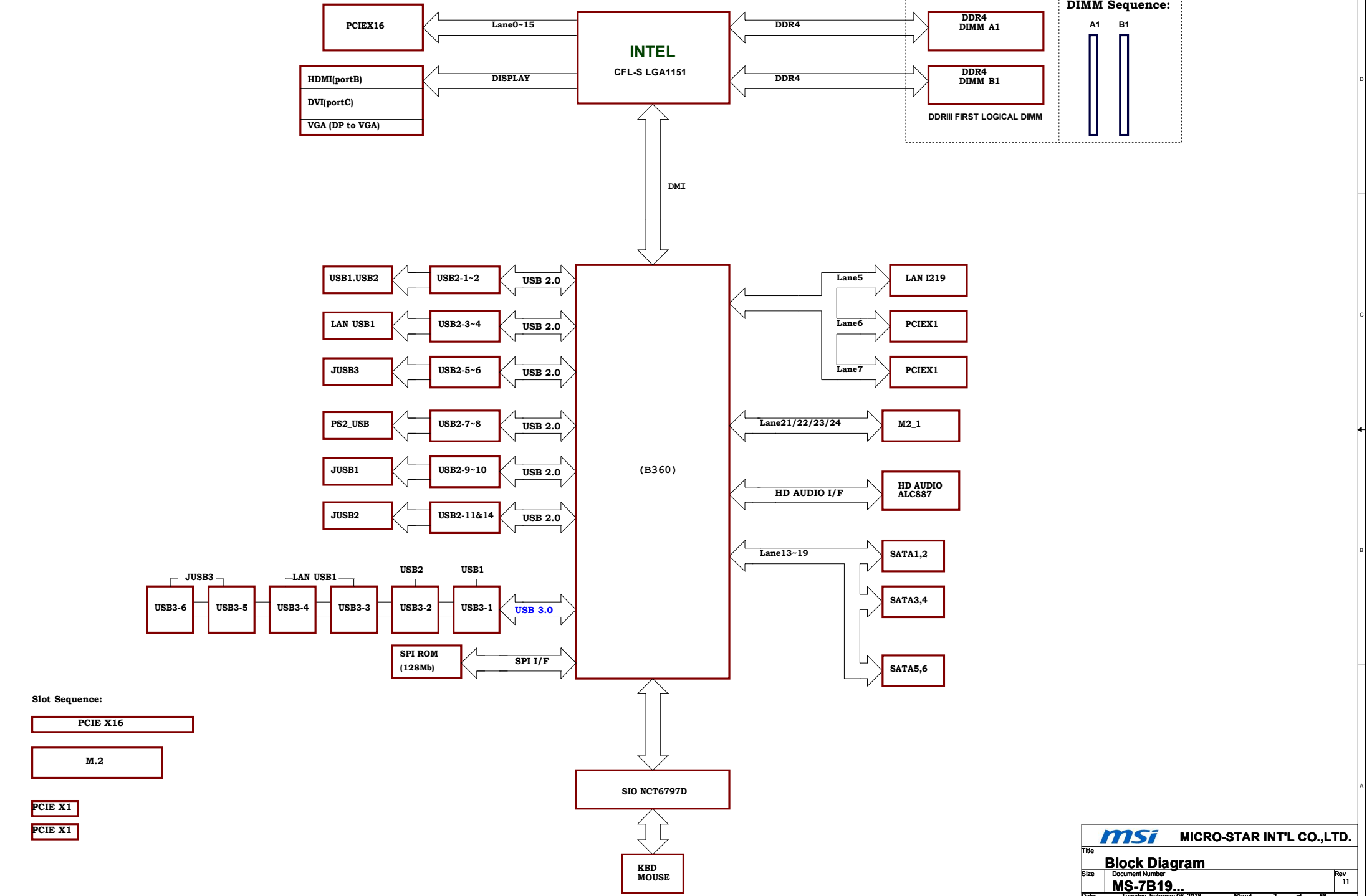
**JCOM1**

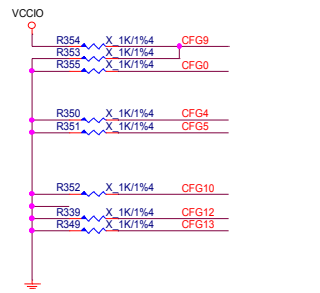
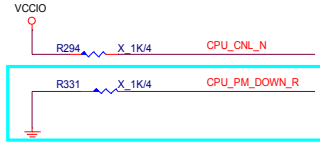
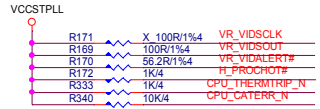
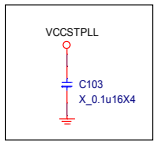
**JTPM1**

**JLPT1**

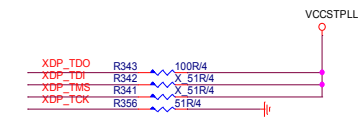
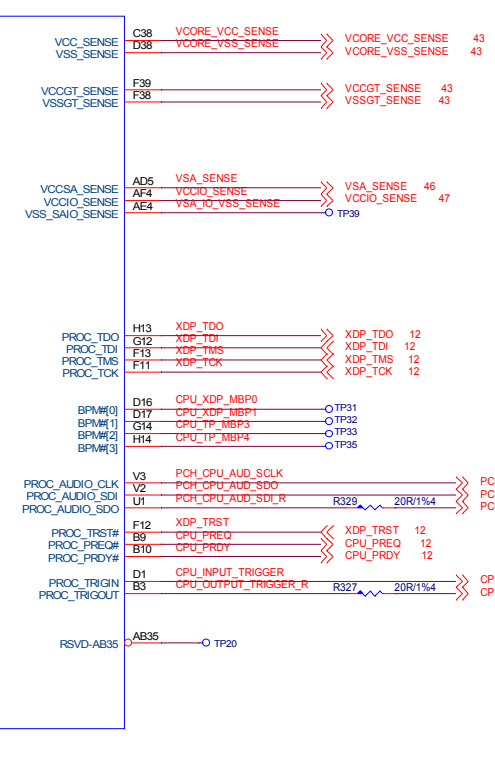
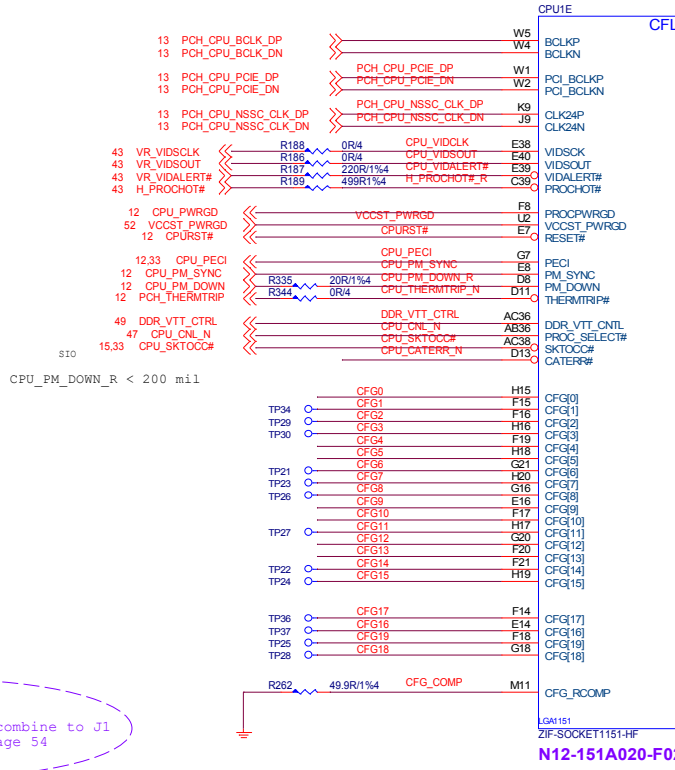
<b>msi</b> MICRO-STAR INT'L CO.,LTD.			
Title <b>Cover Sheet</b>			
Size	Document Number		Rev
	<b>MS-7B19...</b>		<b>11</b>
Date:	Tuesday, February 06, 2018		Sheet 1 of 58

MS-7B19 Block Diagram

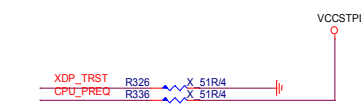




2017/7/13  
Remove JP1 because JP1 combine to J1  
Please see the D78 on page 54



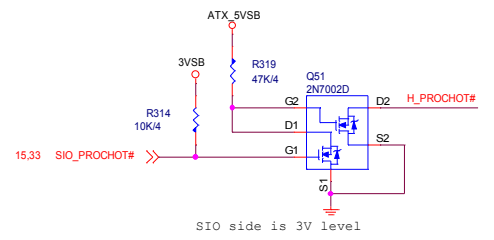
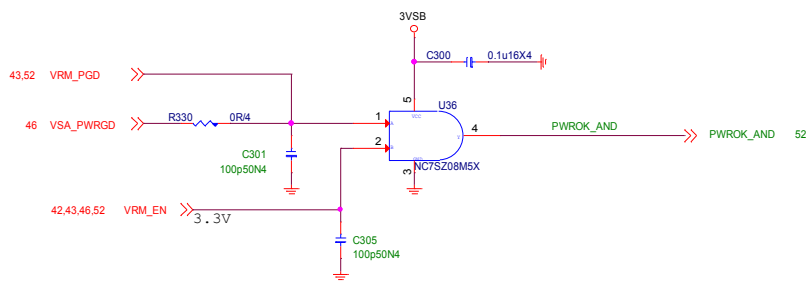
Close CPU <1100 mil  
1000 mil < CPU\_XDP\_MBP0~1 < 6000 mil



## VRM Sequence

11/30 Modify for SILEGO Sequence

MP Remove?



## CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL Lock
1		RSVD	
2	NORM	REVERSE	PEG LANE REVERSAL
3		RSVD	
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CPGSEL(0)
6	DISABLE	ENABLE	PEG0CPGSEL(1)
7	RESET#	BIOS_REQ	PEG DEFER TRAINING
8		RSVD	
9	PRESENT	NO PRESENT	SVID PRESENT
10		RSVD	
11		RSVD	
12		RSVD	
13		RSVD	
14		RSVD	
15		RSVD	
16		RSVD	
17		RSVD	
18		RSVD	
19		RSVD	

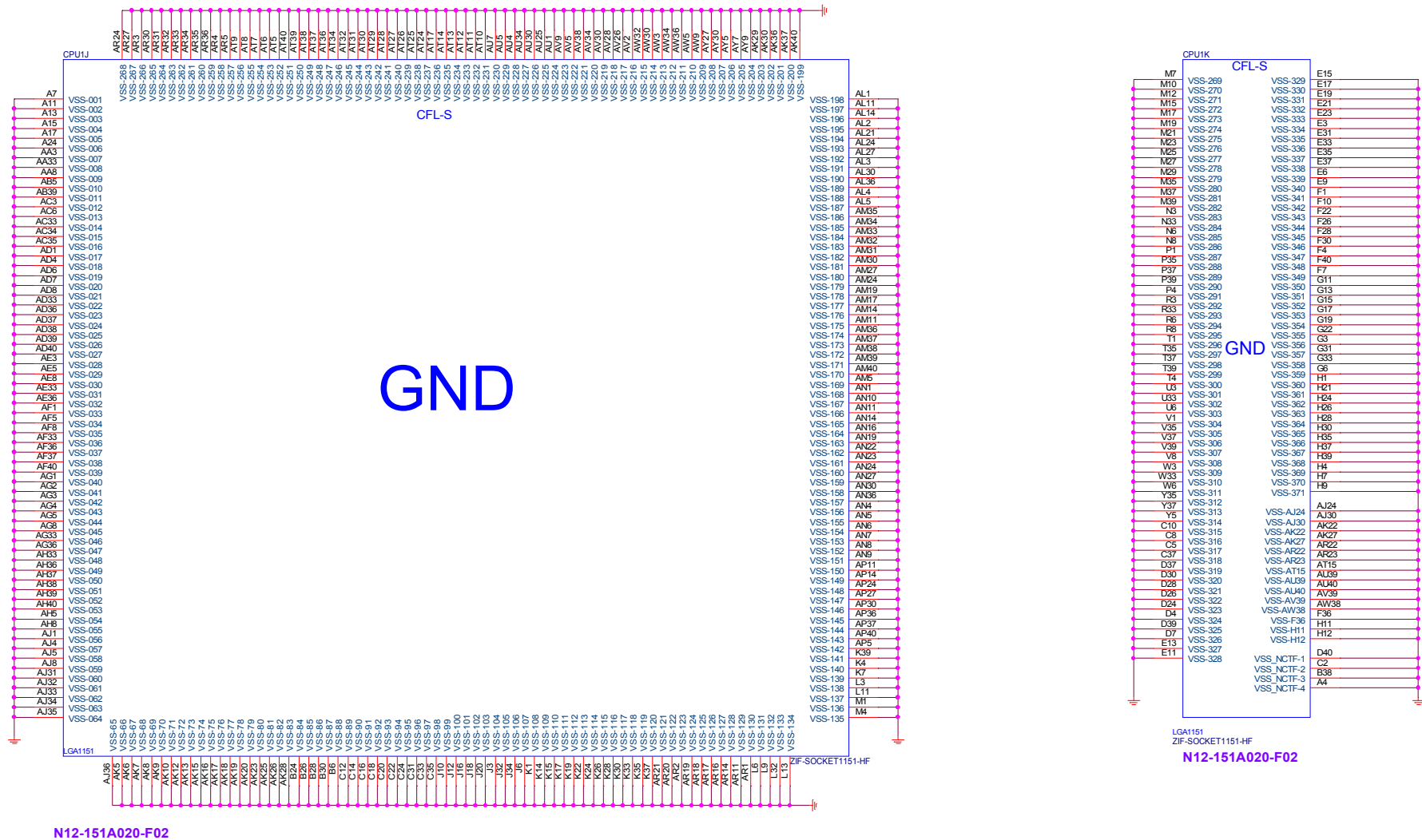
**msi** MICRO-STAR INT'L CO.,LTD.

Title	CPU-Control/MISC/CFG		
Size	Document Number	Rev 11	
	MS-7B19...		
Date	Tuesday, February 06, 2018	Sheet	3 of 58

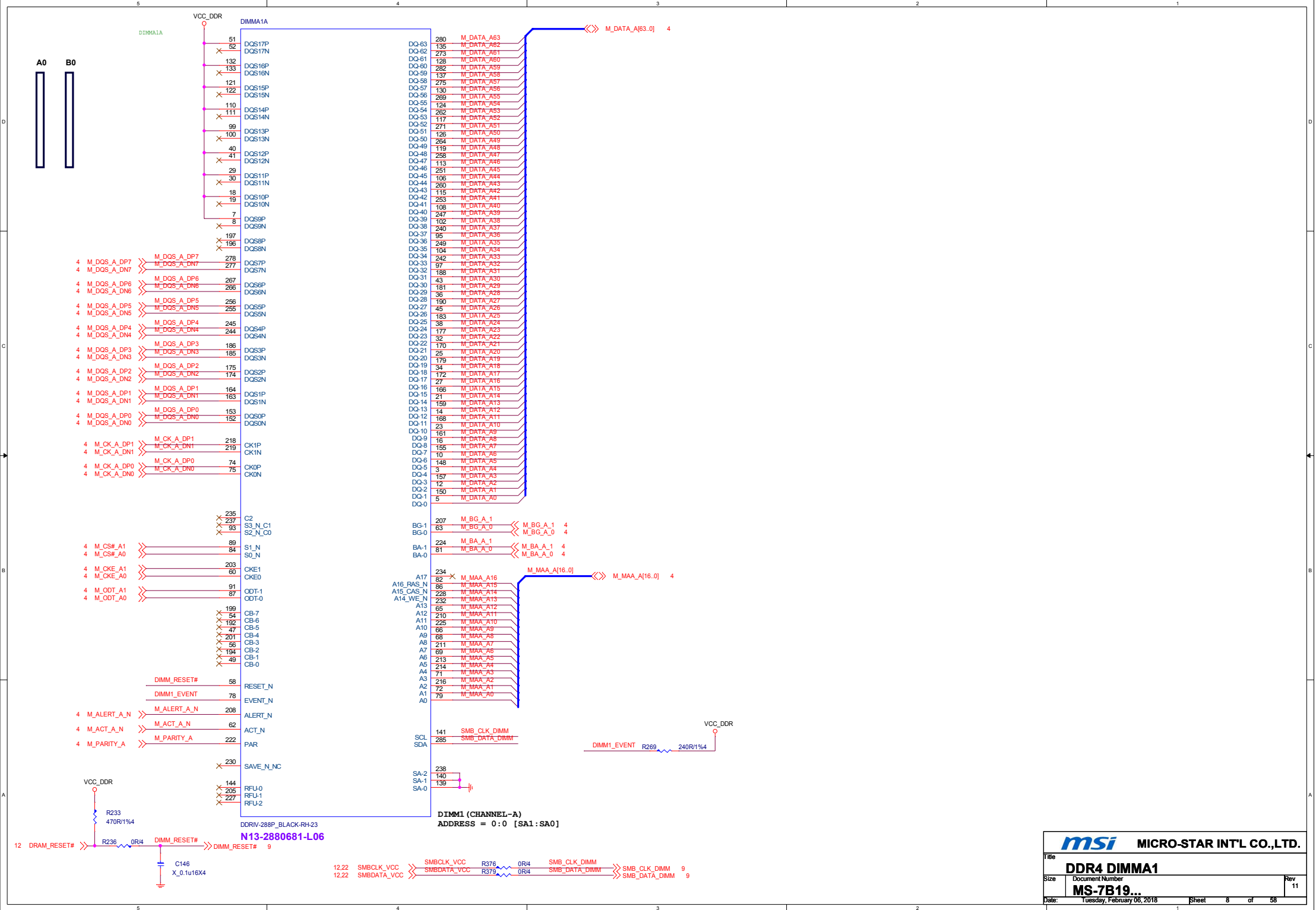








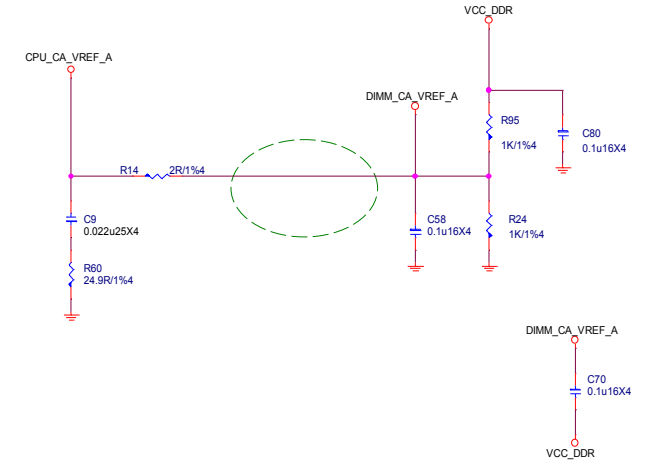
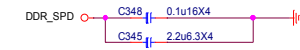
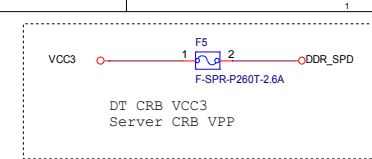
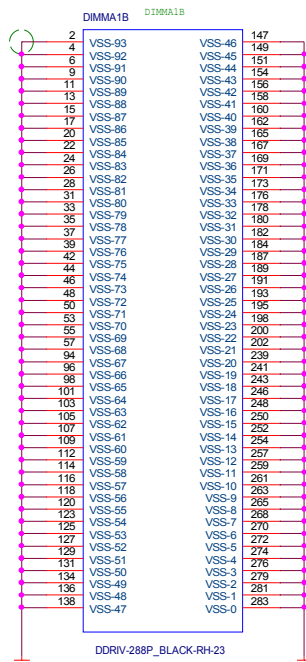
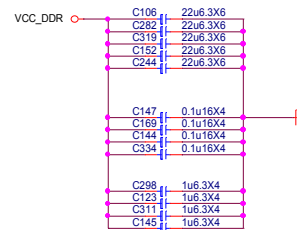
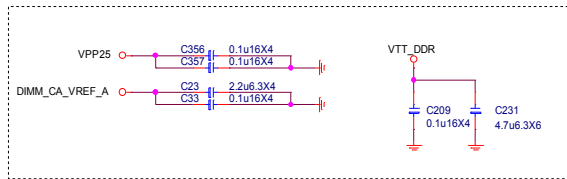
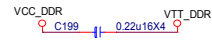


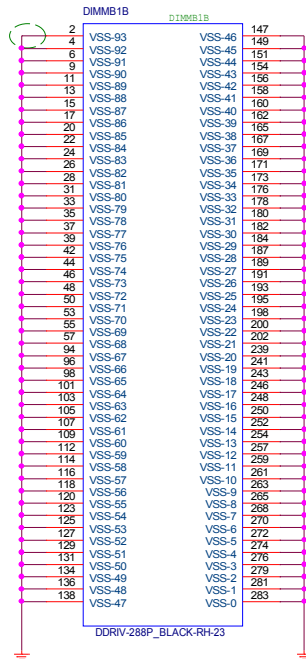
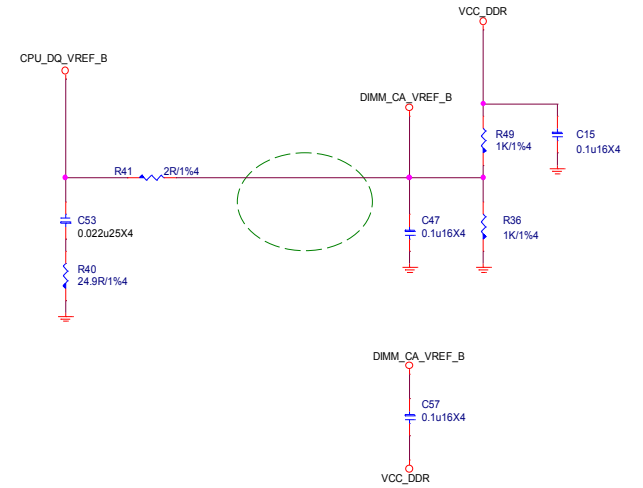
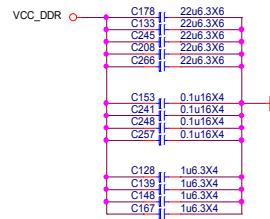
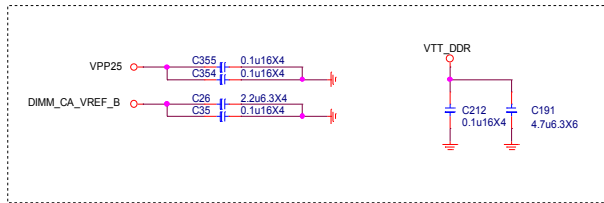
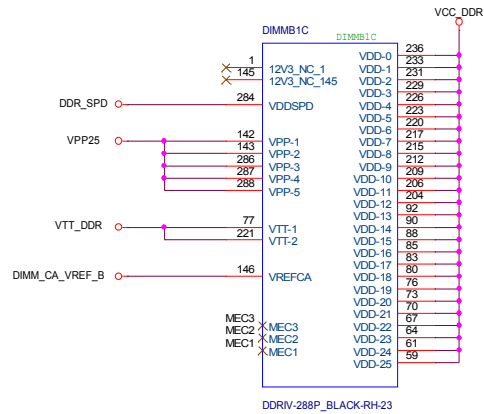






DIMM SLOT PN BY SPEC

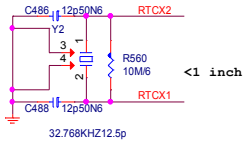




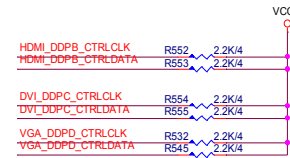
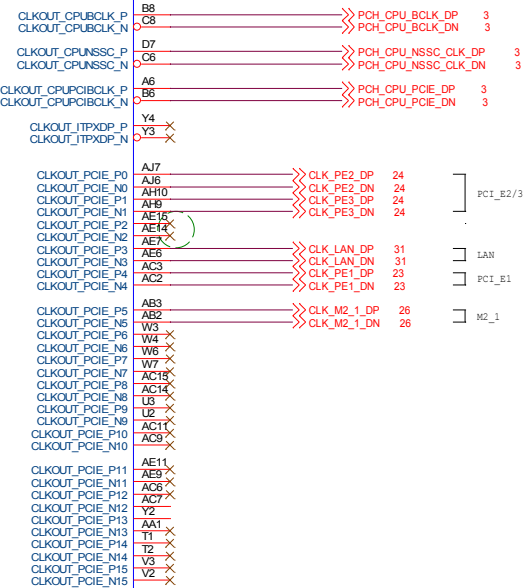
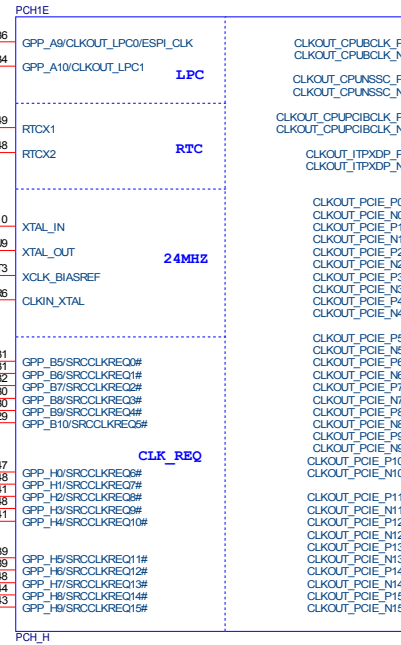
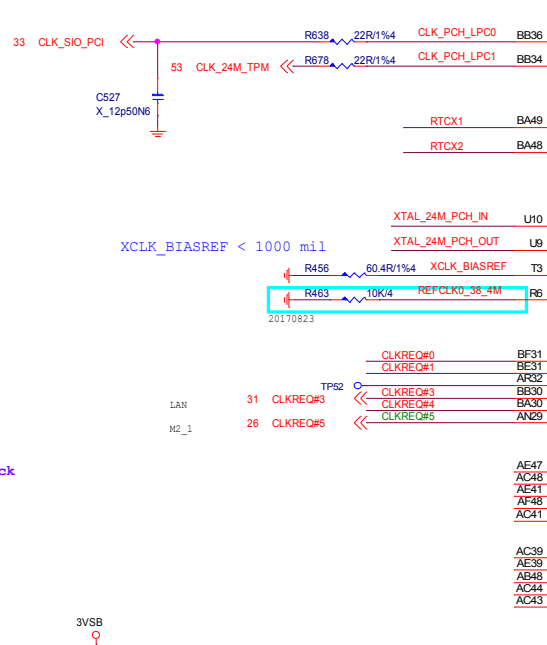
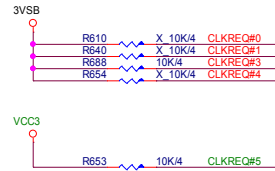
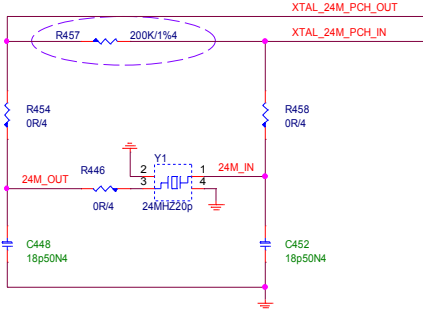


## PCH\_CLK

Close to PCH



2017/7/11  
The value of R689 is the same as PDG r0.9 by Intel's feedback



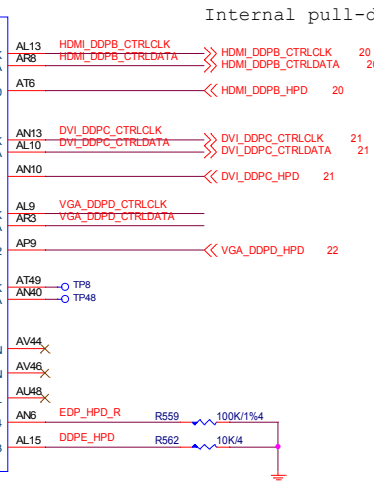
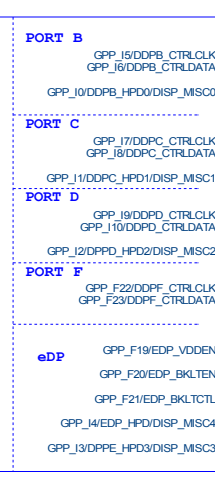
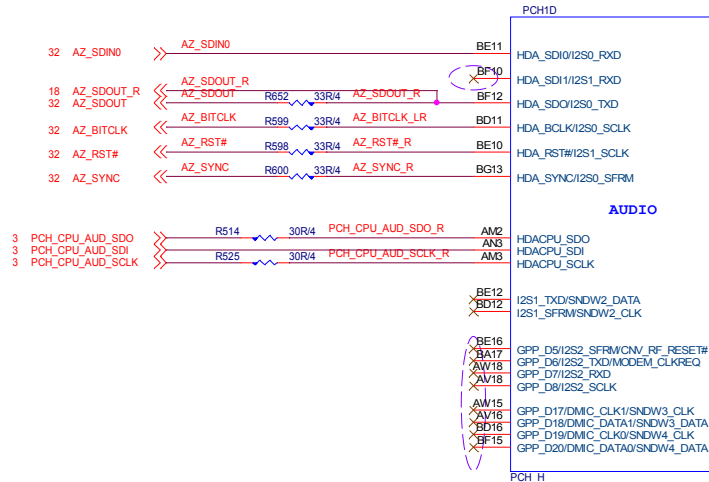
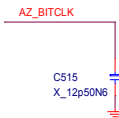
Internal pull-down is disabled after PCH\_PWROK is high.

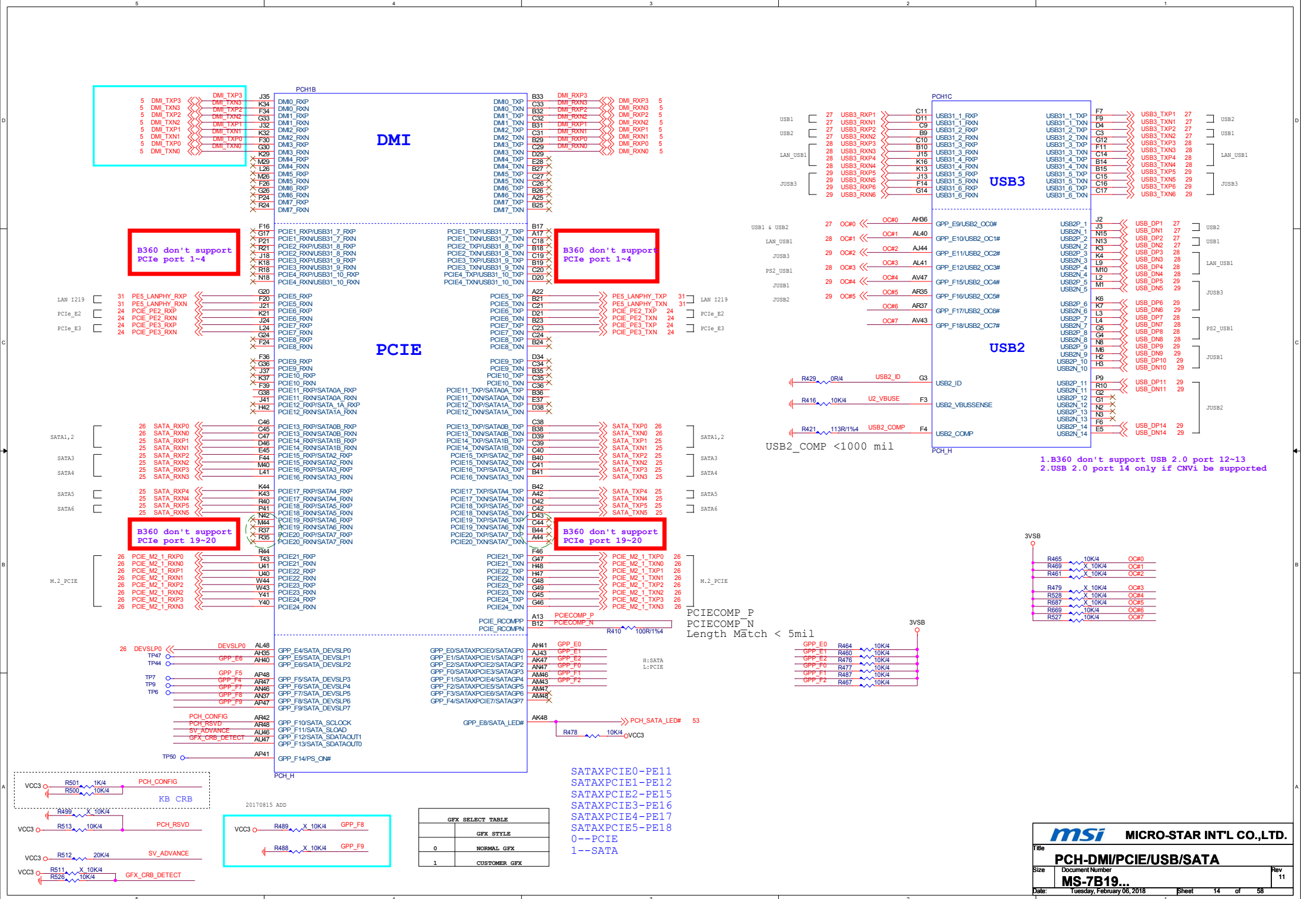
0 : Port B is not detected. (Default)  
1 : Port B is detected.

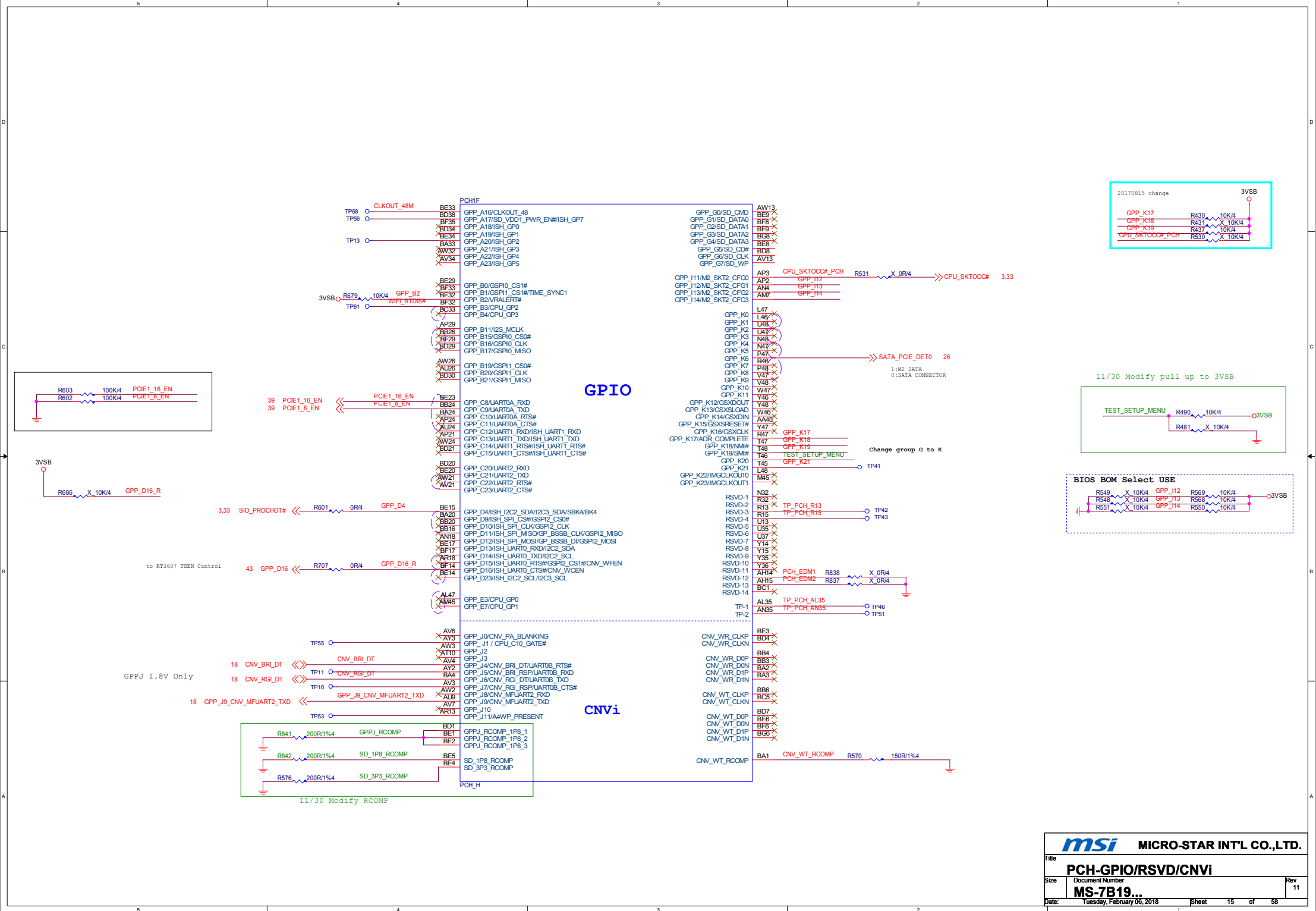
0 : Port C is not detected. (Default)  
1 : Port C is detected.

0 : Port D is not detected. (Default)  
1 : Port D is detected.

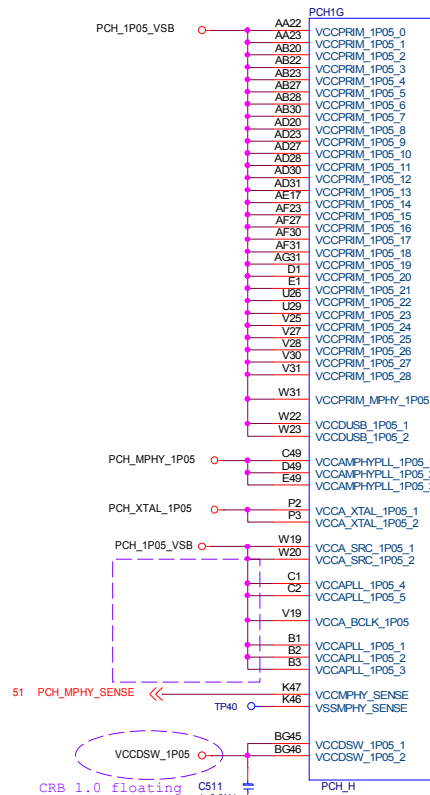
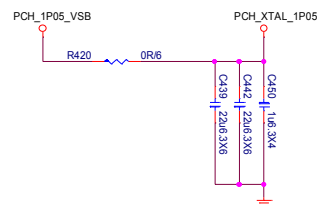
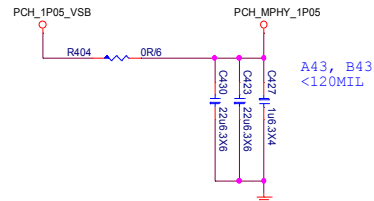
## PCH\_AUDIO



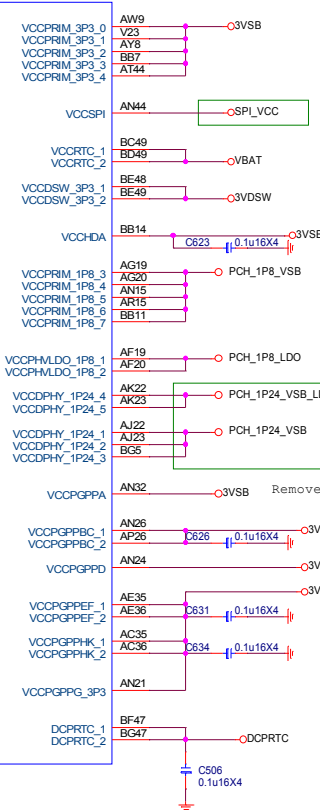




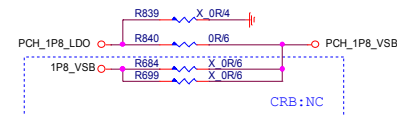
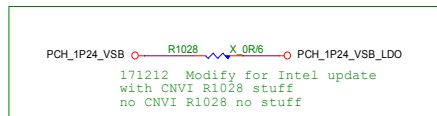




## POWER

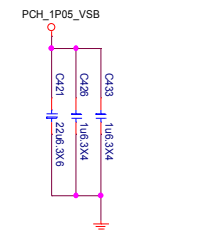


171213 Change to SPI\_VCC

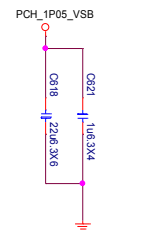


Remove GPPD Colay 1.8V

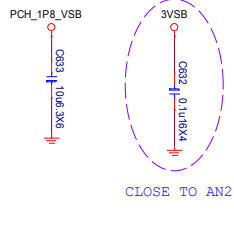
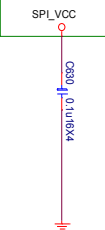
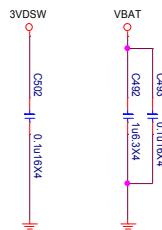
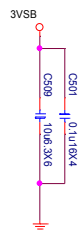
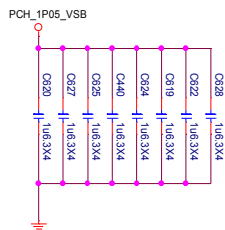
Remove GPPD Colay 1.8V



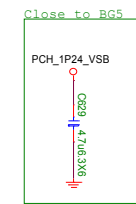
CLOSE TO B1/B2/B3/C1/C2



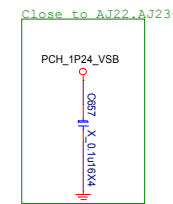
CLOSE TO U26/U29



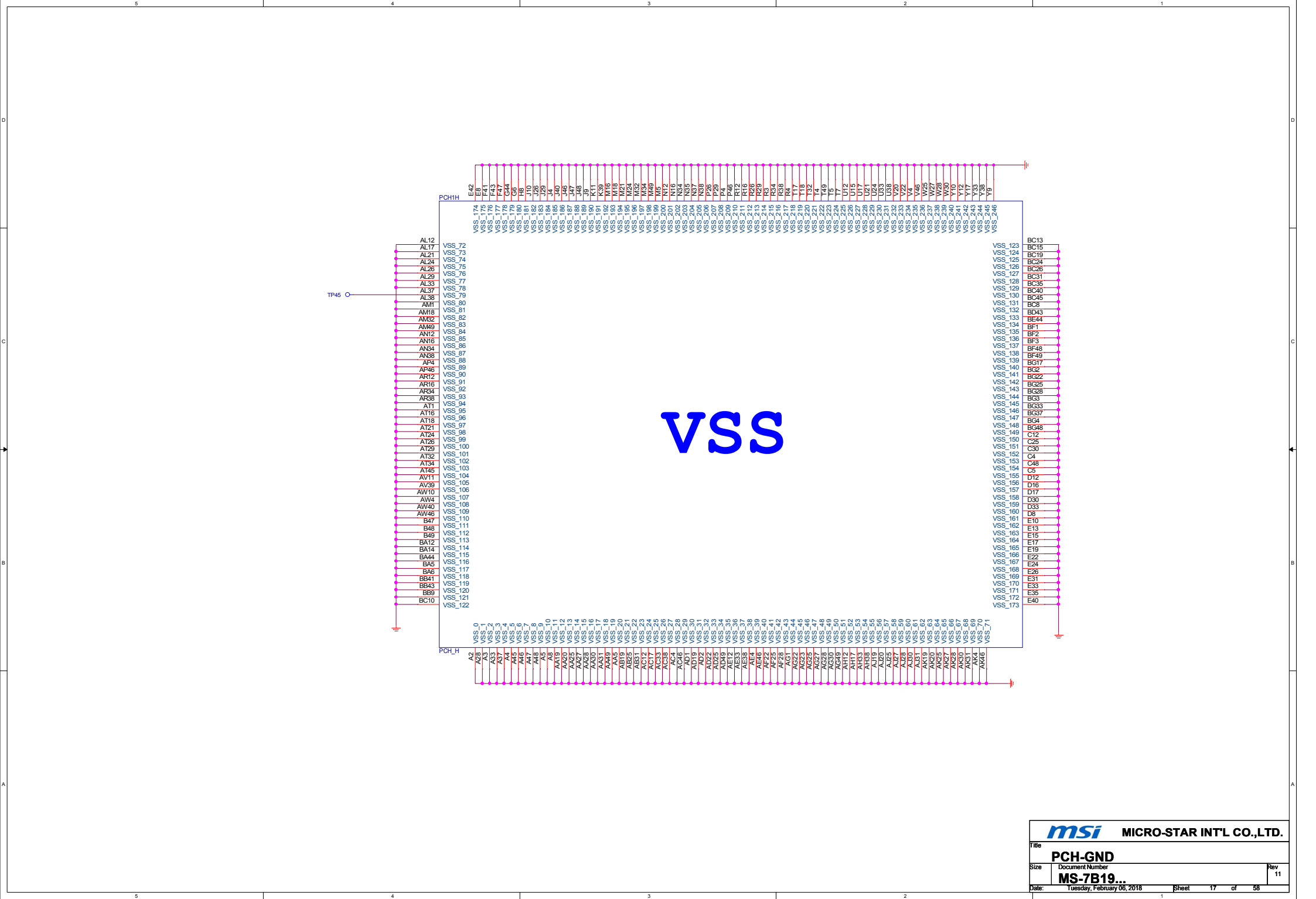
CLOSE TO AN24



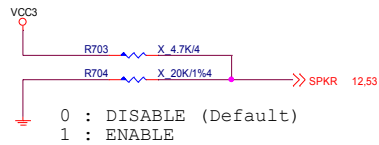
171213 Modify to 4.7uF(PDG)



171213 Reserve for AJ22, AJ23

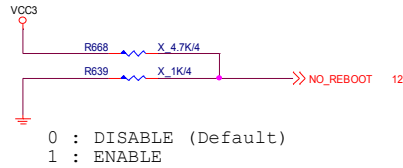


## TOP Swap



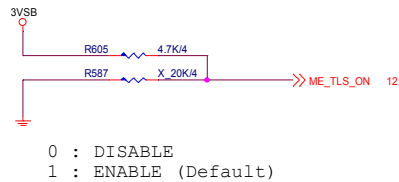
Internal pull-down is disabled after PCH\_PWROK is high.

## No Reboot



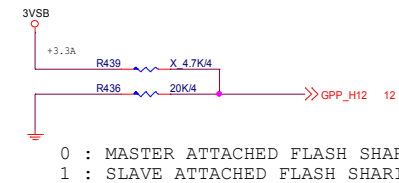
Internal pull-down is disabled after PCH\_PWROK is high.

## TLS confidentiality



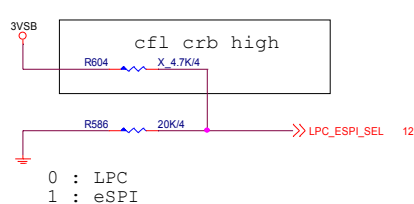
Internal pull-down is disabled after RSMRST# de-assert.

## ESPI FLASH SHARING MODE



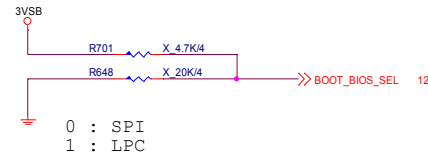
Internal pull-down is disabled after RSMRST# de-assert.

## LPC eSPI Mode



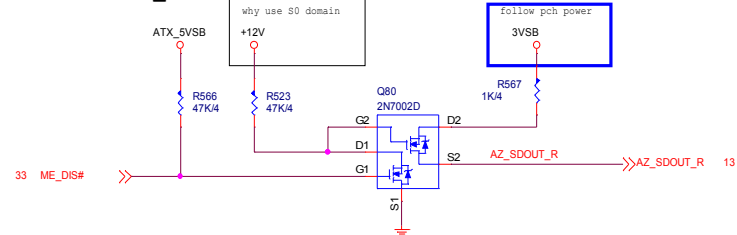
Internal pull-down is disabled after RSMRST# de-assert.

## Boot BIOS



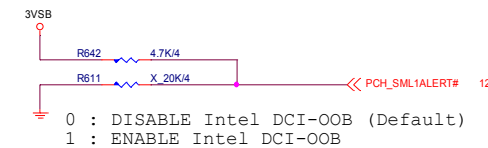
Internal pull-down is disabled after PCH\_PWROK is high.

## HDA\_SDO



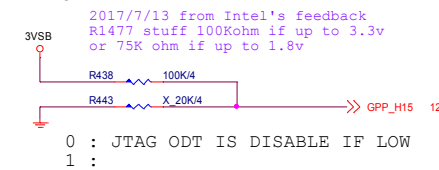
Internal pull-down is disabled after PCH\_PWROK is high.

## DCI ENABLE



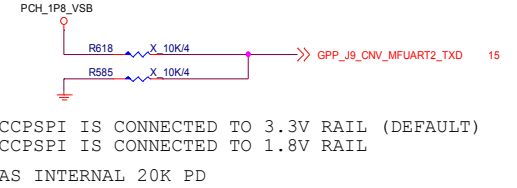
Internal pull-down is disabled after RSMRST# de-assert.

## ODT DISABLE



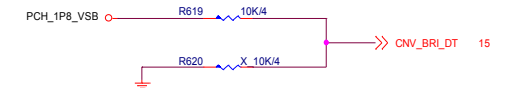
Internal pull-down is disabled after RSMRST# de-assert.

## SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE

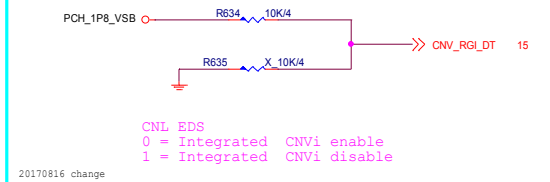


20170814 CHANGE

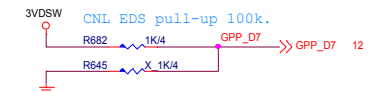
## XTAL FREQUENCY SELECTION



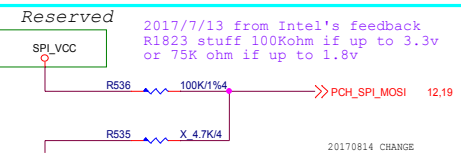
## MODEM AND NFC REFERENCE CLOCK SOURCE SELECT



## XTAL INPUT MODE

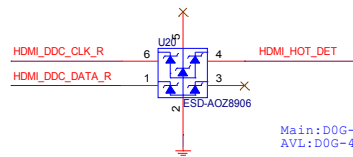
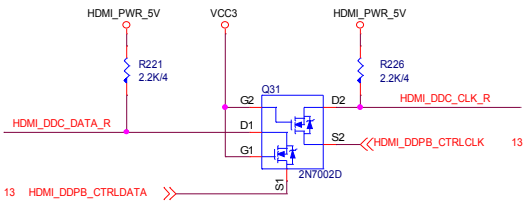
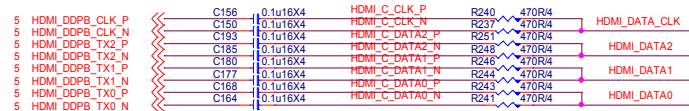


171213 Change to SPI\_VCC

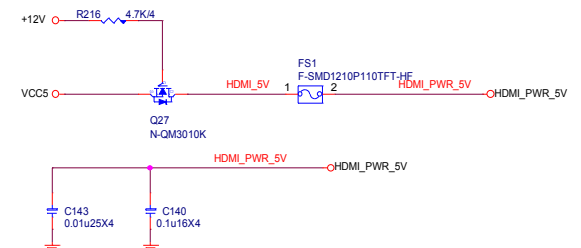
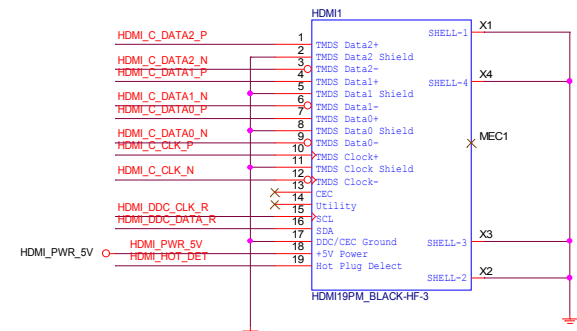
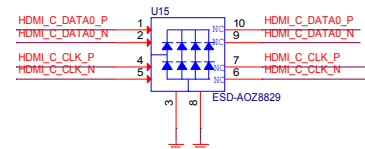
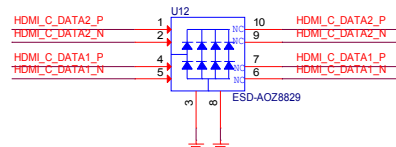
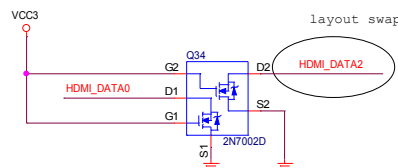
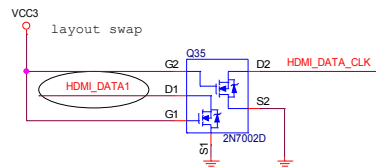




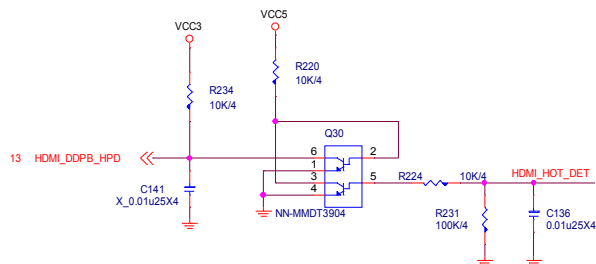
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



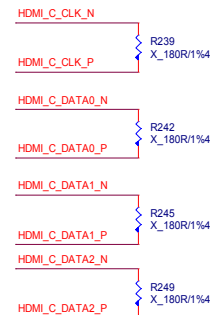
Main:D0G-05A0529-A68  
AVL:D0G-45B0510-II14



HPD



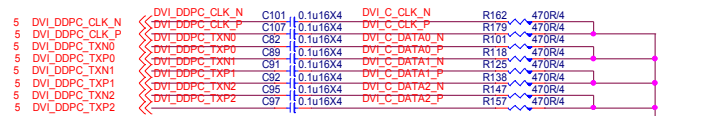
For EMI



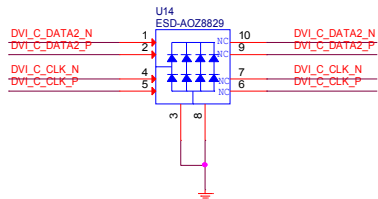
msi MICRO-STAR INT'L CO.,LTD.

Title	HDMI Connector		
Size	Document Number	Rev	
	MS-7B19...	11	
Date	Tuesday, February 06, 2018	Sheet	20 of 58

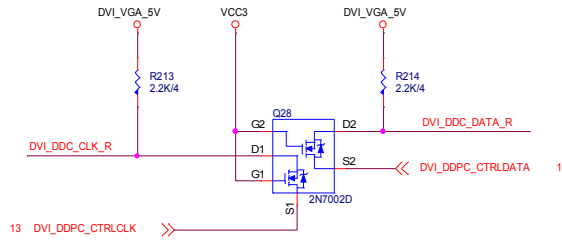
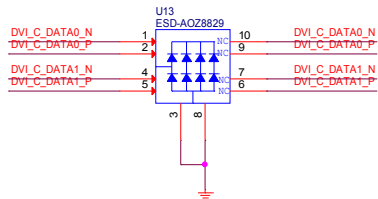
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



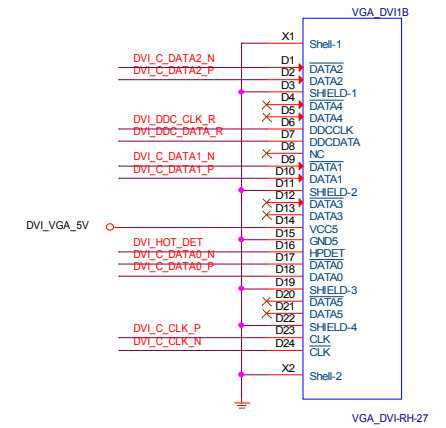
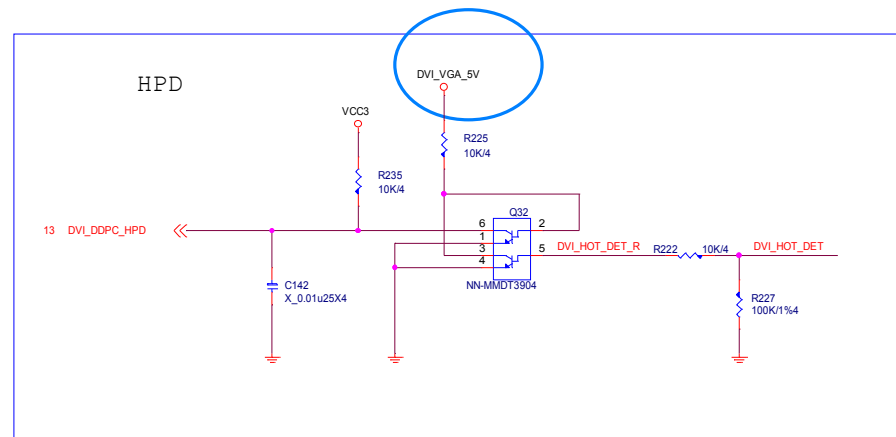
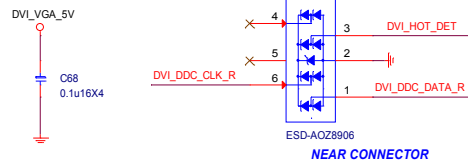
U26 AVL:D0G-05A050C-005  
D0G-06A050C-A68



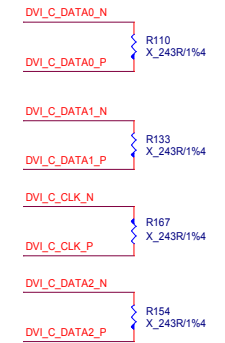
U27 AVL:D0G-05A050C-005  
D0G-06A050C-A68



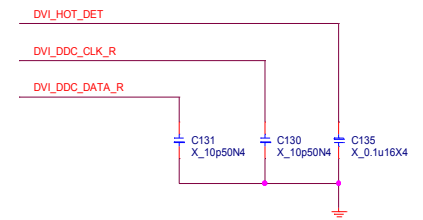
EMI Cap near connector DVI1




For EMI

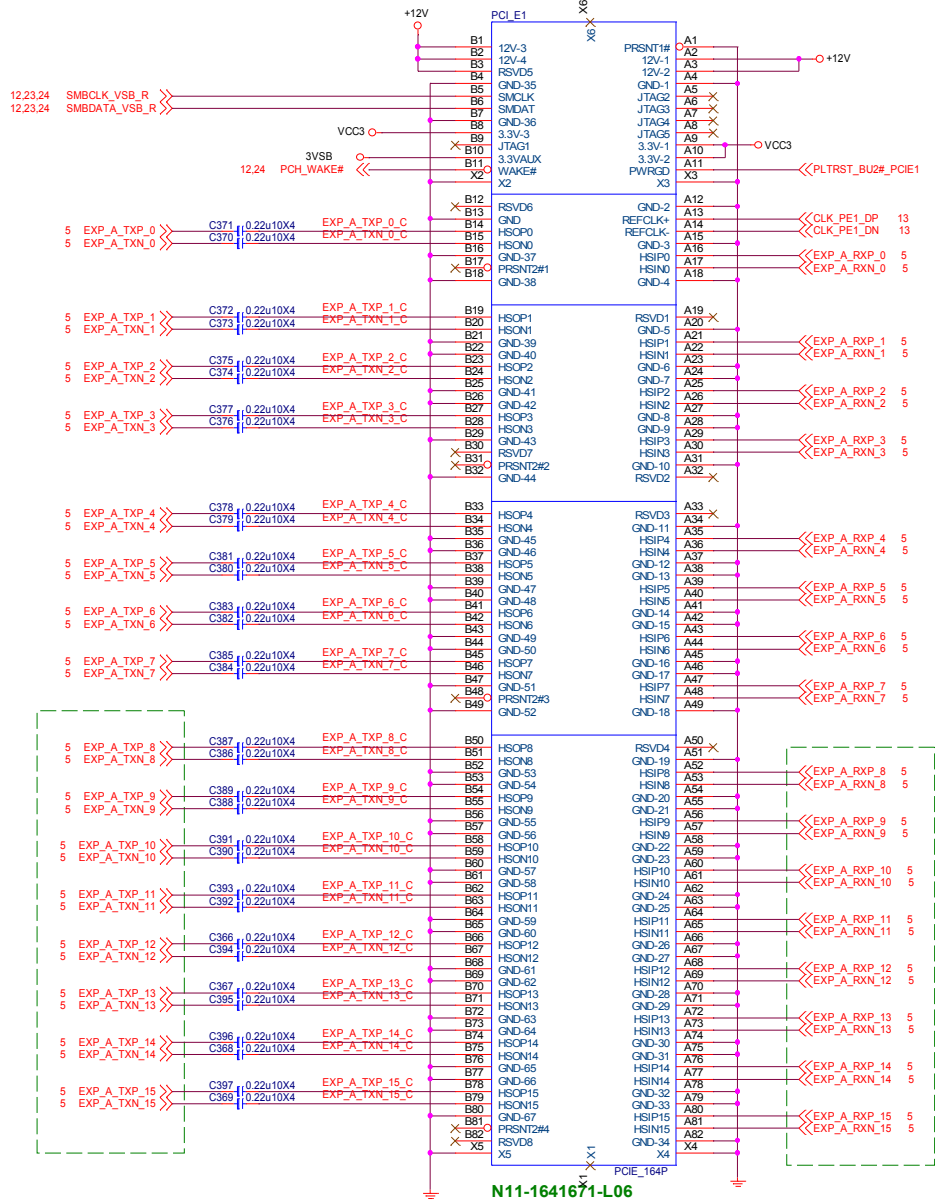


EMI

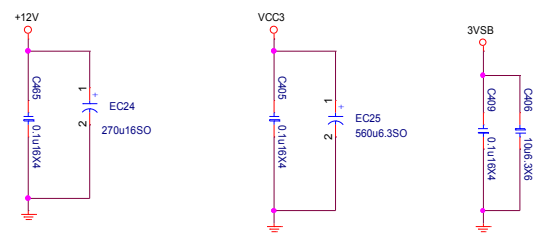
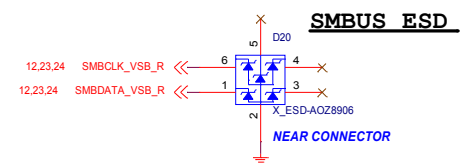


 <b>MICRO-STAR INT'L CO.,LTD.</b>	
Title	
<b>VGA - RTD2166</b>	
Size	Document Number <b>MS-7B19...</b>
Date:	Tuesday, February 06, 2018         Sheet 22 of 58         Rev 11



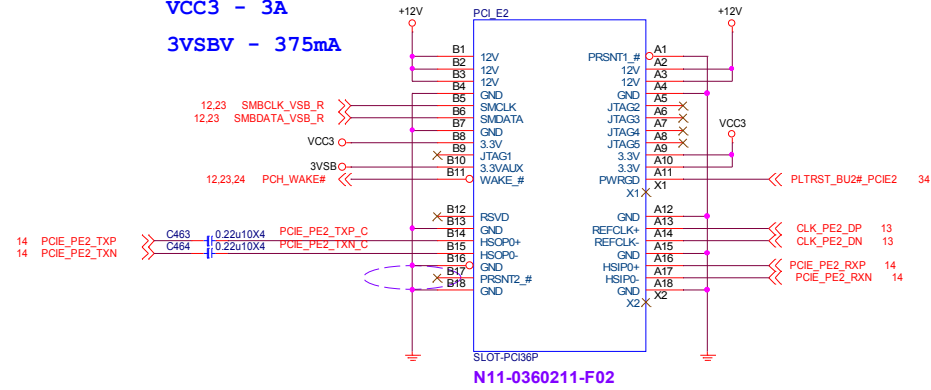


5.5A at +12V  
3A at VCC3  
375mA at 3VSB

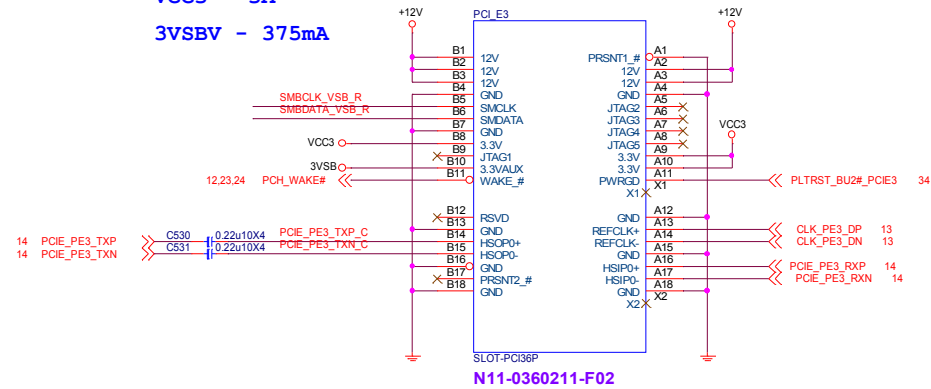


# PCH PCIE X1 Slot

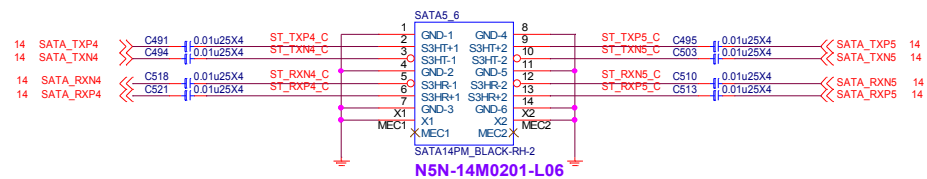
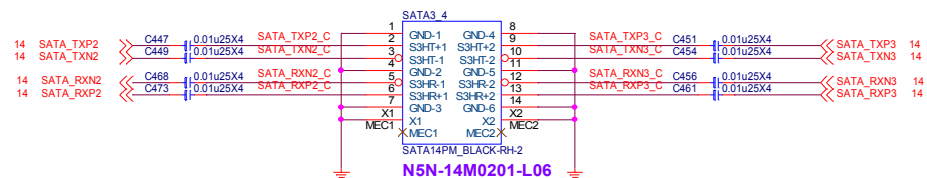
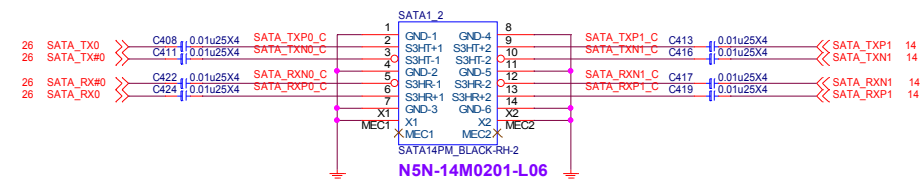
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



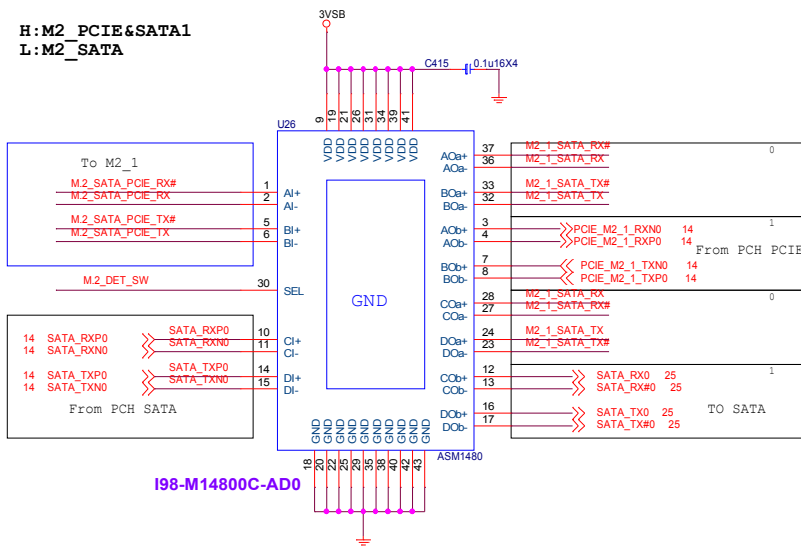
12V - 0.5A  
VCC3 - 3A  
3VSBV - 375mA



From SWITCH



H:M2\_PCIE&SATA1  
L:M2\_SATA

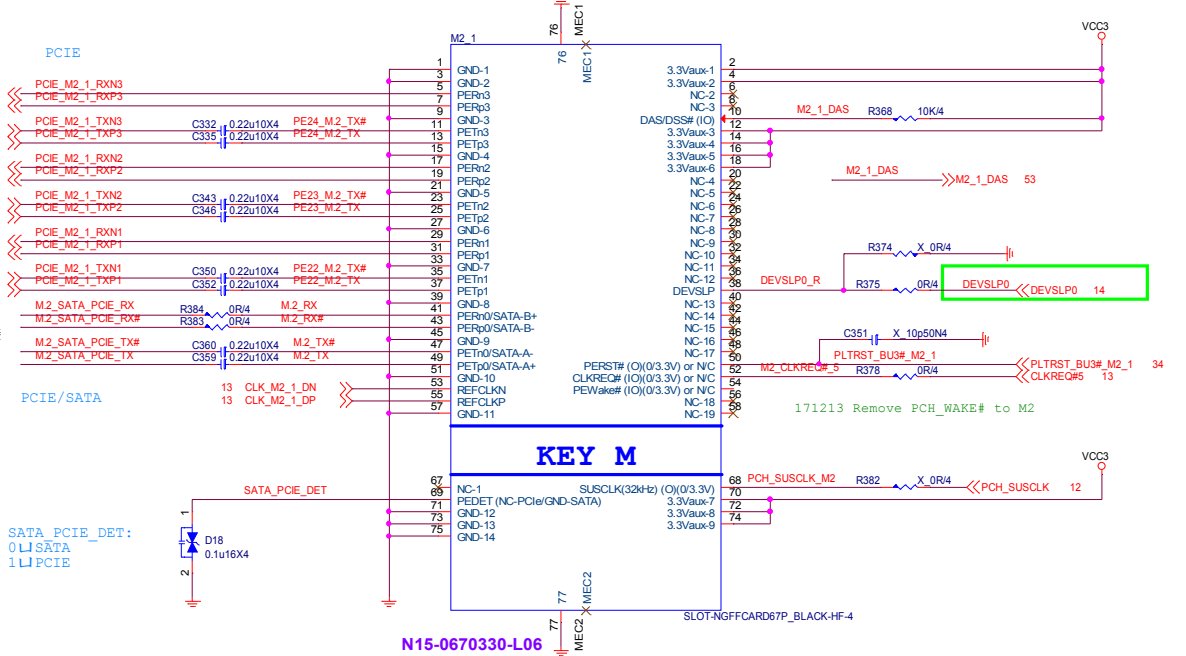


I98-M14800C-AD0

PCIE  
14 PCIE\_M2\_1\_RXN3  
14 PCIE\_M2\_1\_RXP3  
14 PCIE\_M2\_1\_TXN3  
14 PCIE\_M2\_1\_TXP3  
14 PCIE\_M2\_1\_RXN2  
14 PCIE\_M2\_1\_RXP2  
14 PCIE\_M2\_1\_TXN2  
14 PCIE\_M2\_1\_TXP2  
14 PCIE\_M2\_1\_RXN1  
14 PCIE\_M2\_1\_RXP1  
14 PCIE\_M2\_1\_TXN1  
14 PCIE\_M2\_1\_TXP1

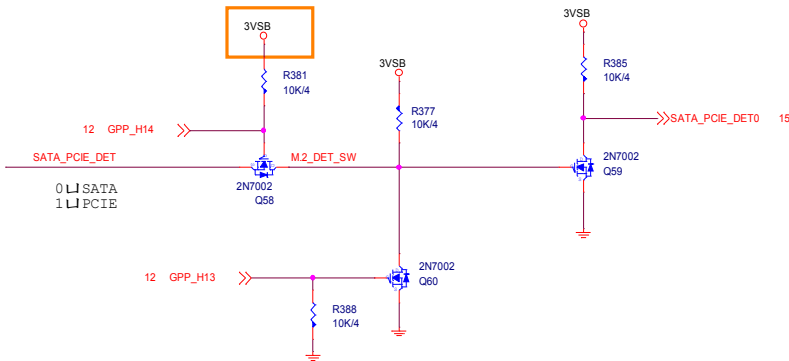
SATA 要反接

PCIE/SATA  
SATA\_PCIE\_DET:  
0 L SATA  
1 L PCIE



N15-0670330-L06

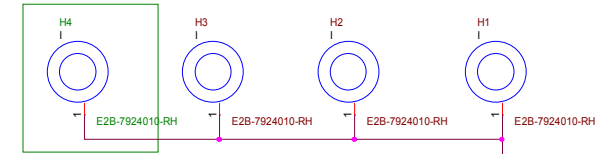
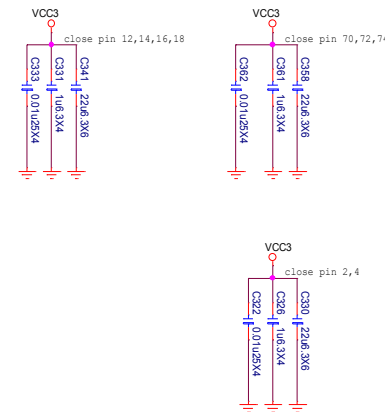
H:M2\_SATA  
L:M2\_PCIE&SATA1



BIOS\_MODE

GPP_H14	GPP_H13	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI (1)	GPI (0)	AUTO

	GPP_K6
0	SATA1 M2_1_PCIE
1	M2_1_SATA

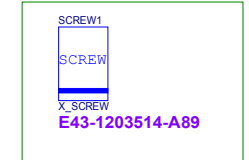


E2B-7B05010-A89

11/30 Add H4 for PM SPEC to support 110



E2B-7984020-A89

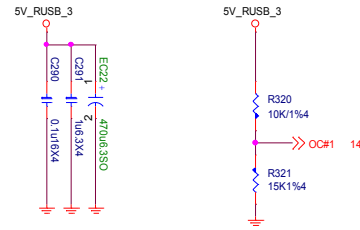
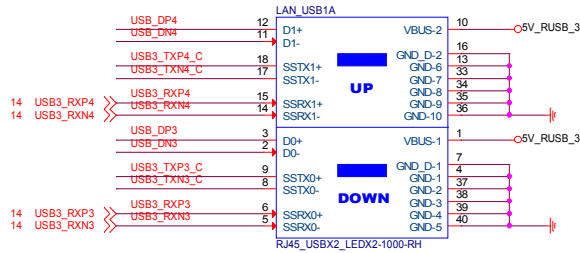
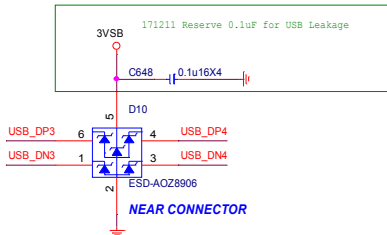
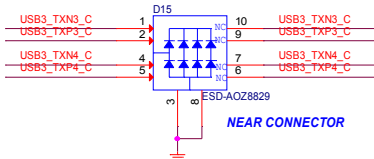
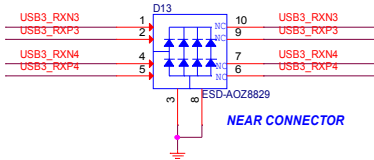


E43-1203514-A89

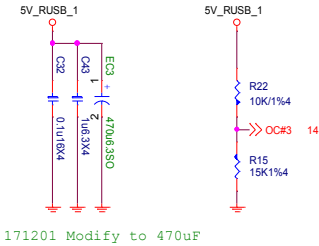
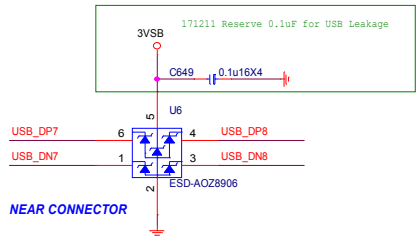
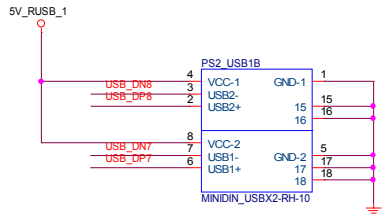
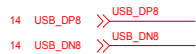
171219 Remove BOM for PM SPEC



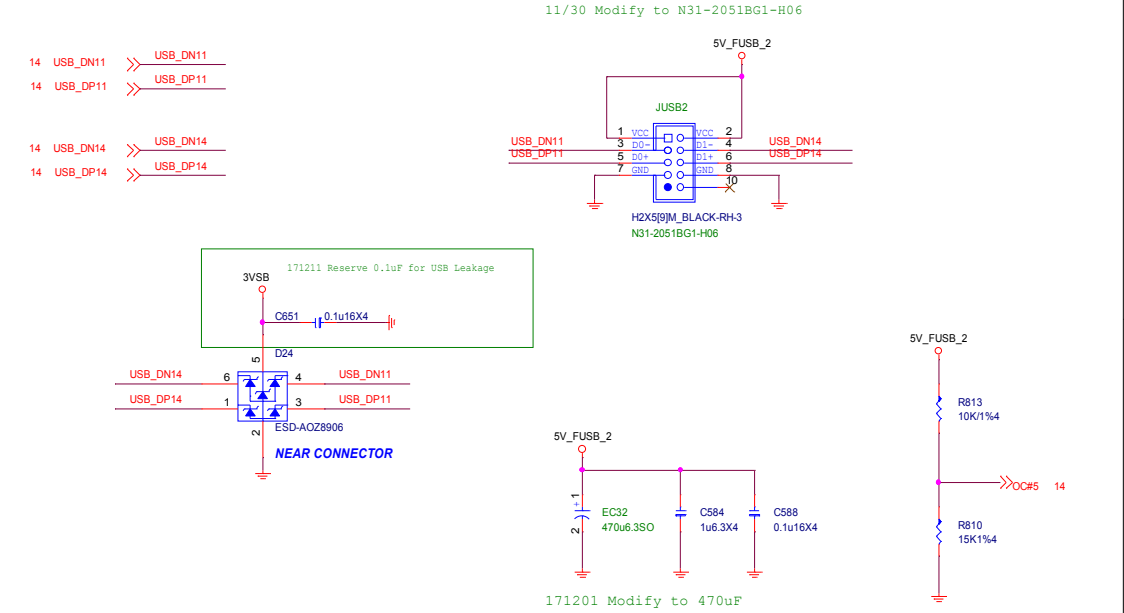
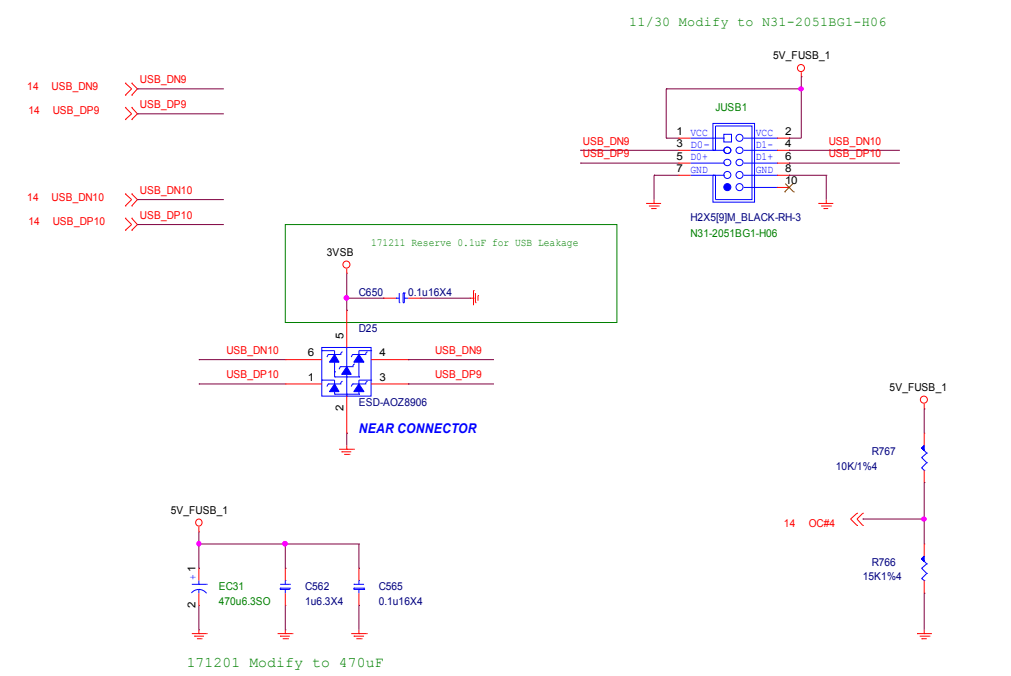
LAN\_USB1



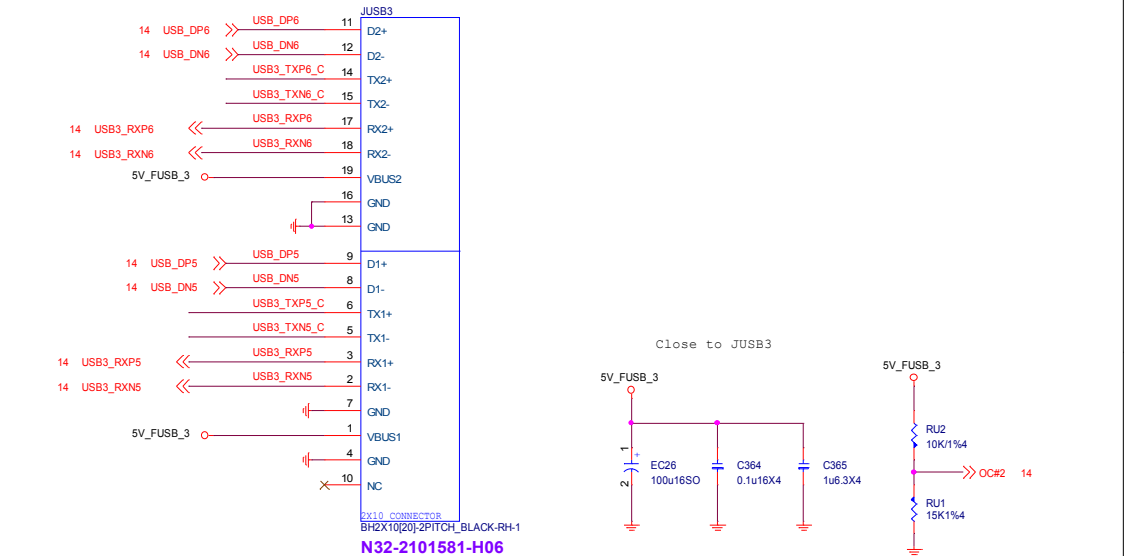
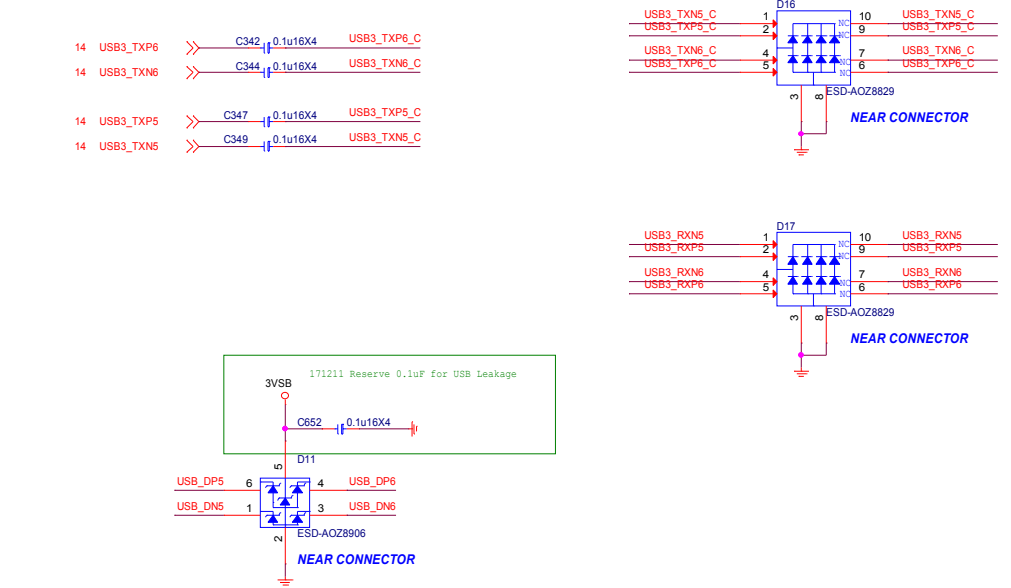
PS2\_USB1



FRONT USB2.0



FRONT USB3.0  
180

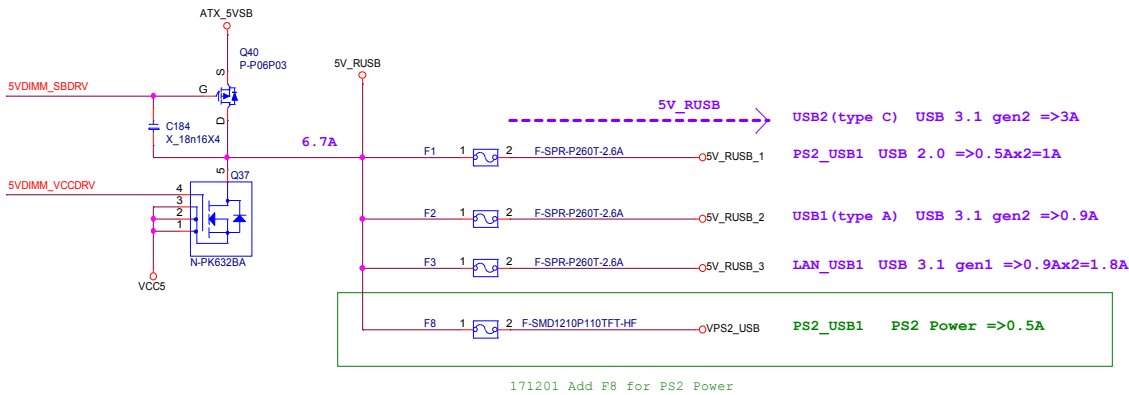




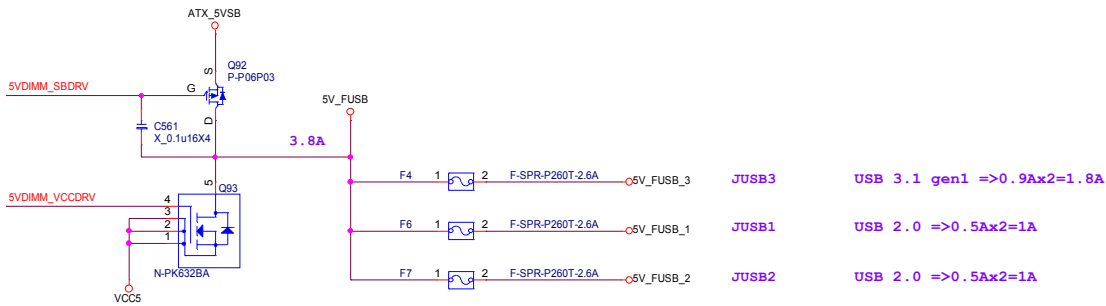
USB POWER

41 5VDIMM\_SBDRV << 5VDIMM\_SBDRV  
41 5VDIMM\_VCCDRV << 5VDIMM\_VCCDRV

REAR USB PORT POWER

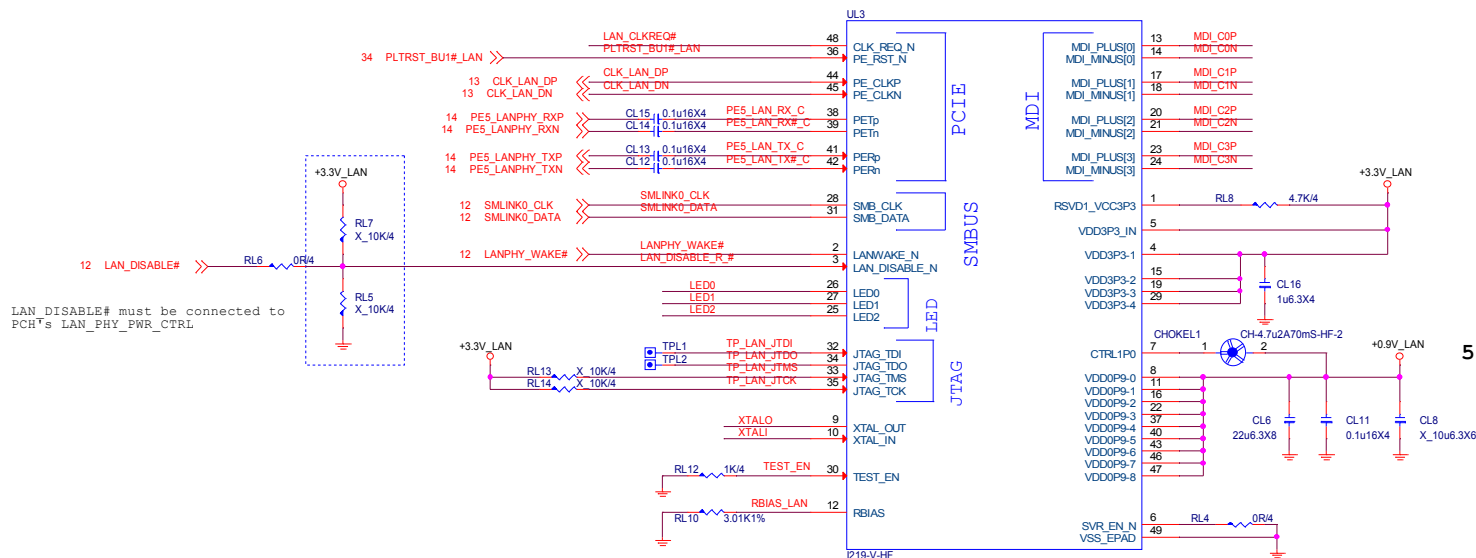


FRONT USB PORT POWER

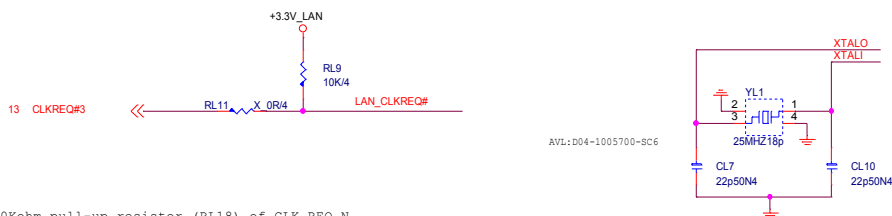


Intel Lan- i219

8111H:B06-08111CC-R09  
8111G:B06-081116C-R09

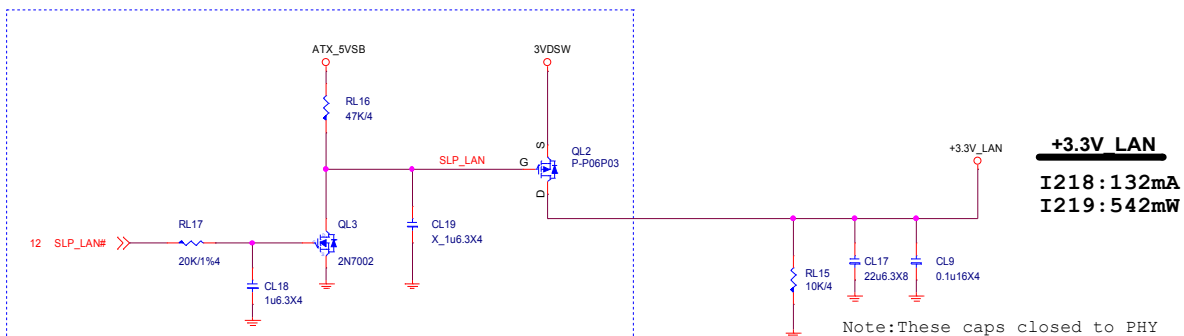


PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port.  
If CLK REQ N is not used, pin48 is pulled up 10K $\Omega$  to 3.3V LAN



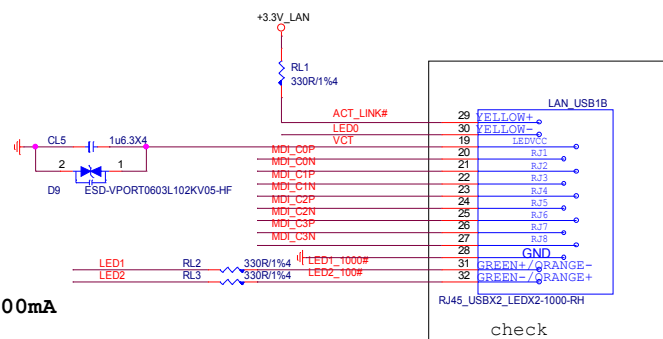
The 10Kohm pull-up resistor (RL18) of CLK\_REQ\_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:  
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.

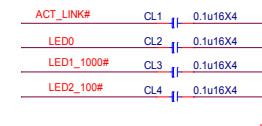


Note: These caps closed to PHY

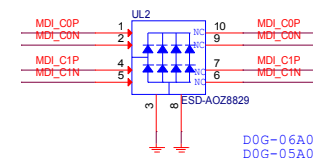
### LAN Connector



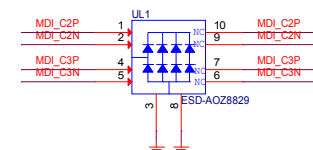
*For EMI*



UL2&UL3 close to connector

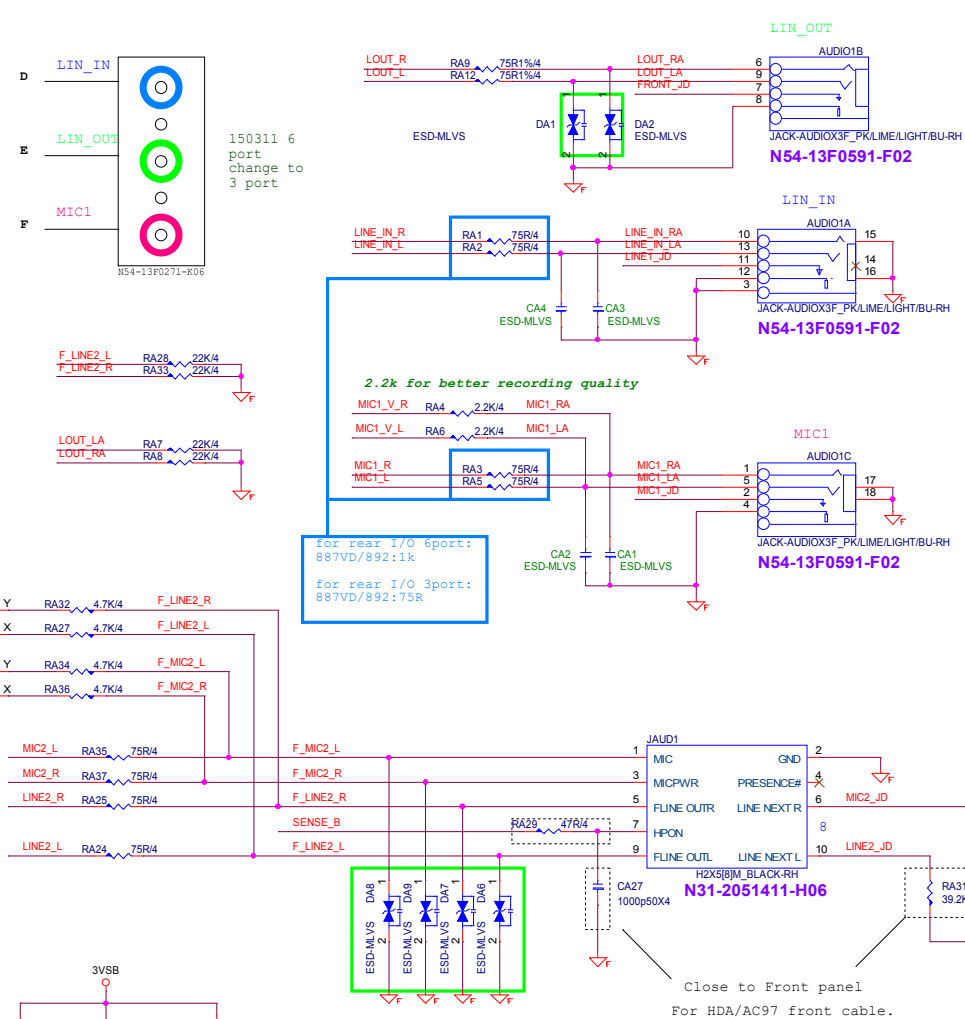
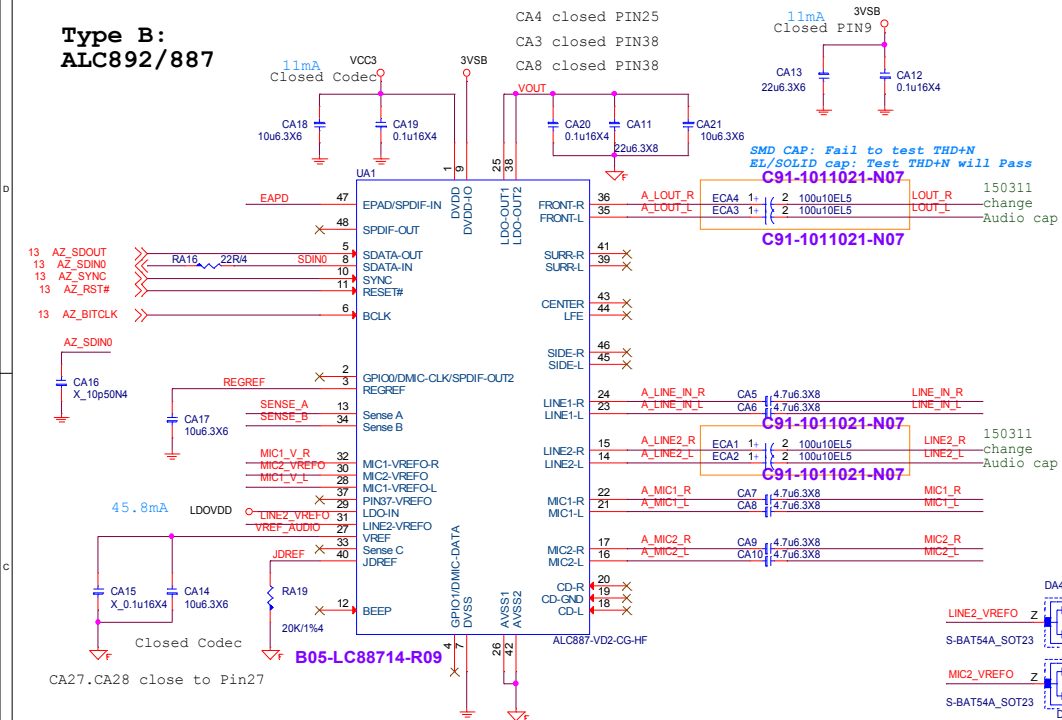


D0G-06A050C-A68  
D0G-05A0300-I14



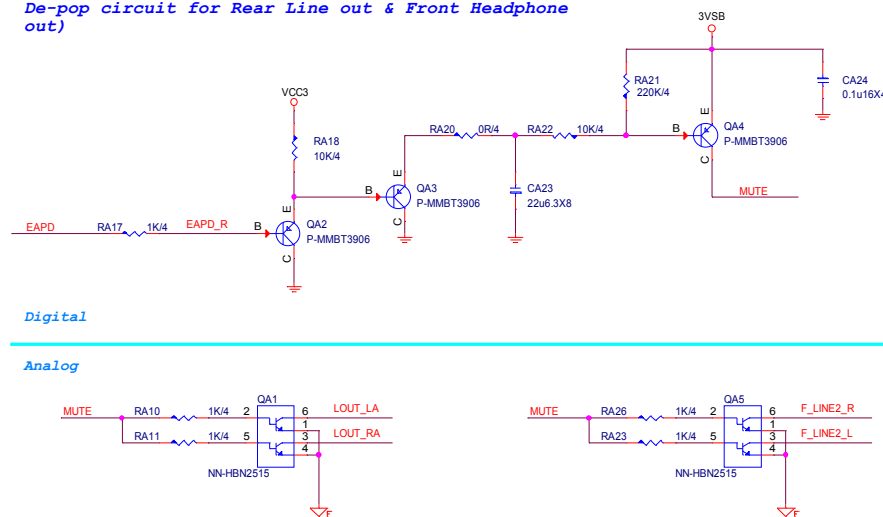
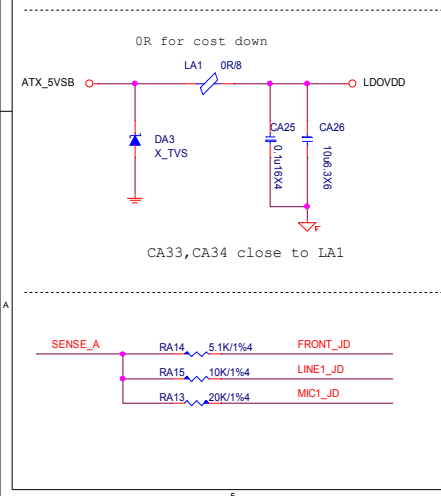
Do not pair MDI0 and MDI1 on the same TVSdevice  
(avoid LAN POE connecting issue).  
Otherpairing combination is ok.

Type B:  
ALC892/887



### Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)



Varister --> cap for cost down  
D0G-2950500-SI0  
D0G-3010510-I05  
Close to Jack

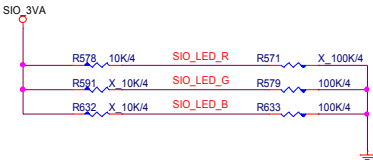


33 PLTRST\_BU1# >> R629 100R/1%4 PLTRST\_BU1#\_LAN 31

33 PLTRST\_BU2# >> R651 100R/1%4 PLTRST\_BU2#\_PCIE1 23  
R650 100R/1%4 PLTRST\_BU2#\_PCIE2 24  
R627 100R/1%4 PLTRST\_BU2#\_PCIE3 24

33 PLTRST\_BU3# >> R667 100R/1%4 PLTRST\_BU3#\_M2\_1 26  
R672 100R/1%4 PLTRST\_BU3#\_TPM 53

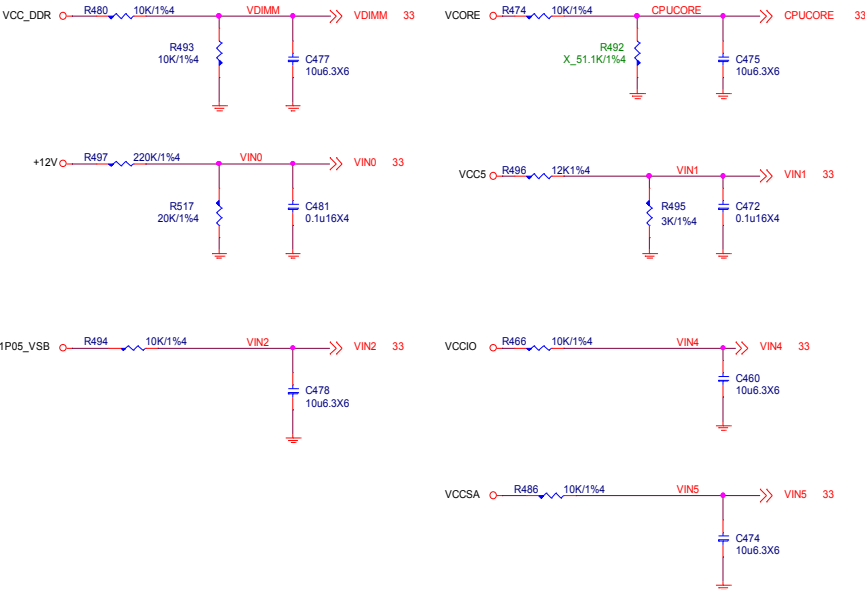
33,38,39 SIO\_LED\_G >>  
33,38,39 SIO\_LED\_B >>  
33,38,39 SIO\_LED\_R >>



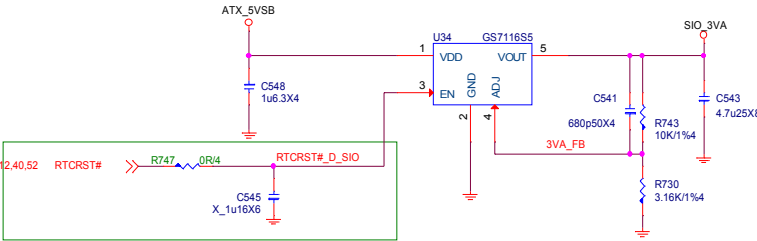
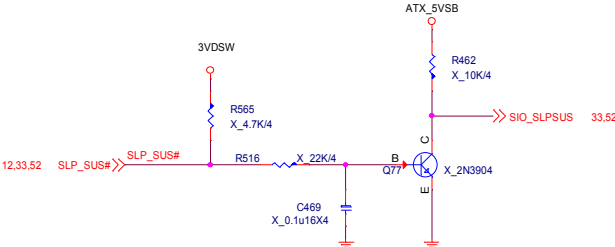
11/30 Remove PCH\_1P05\_VSB to RSMRST# Circuit

## HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect

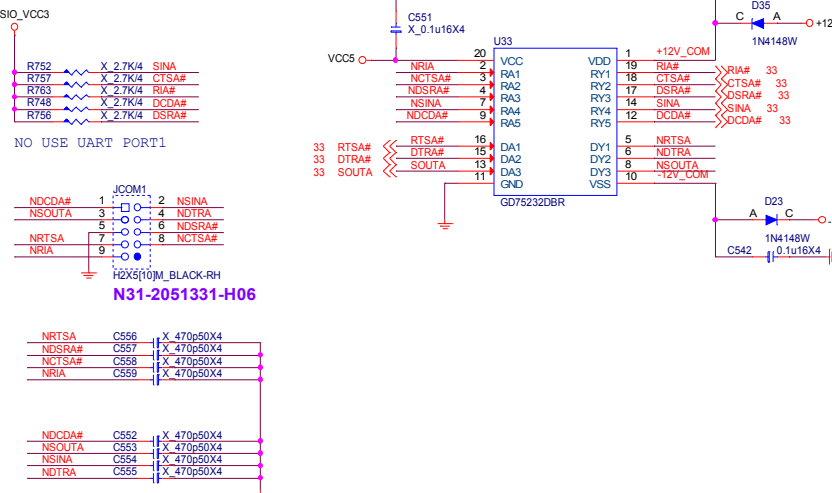


## SLP\_SUS Co-lay circuit

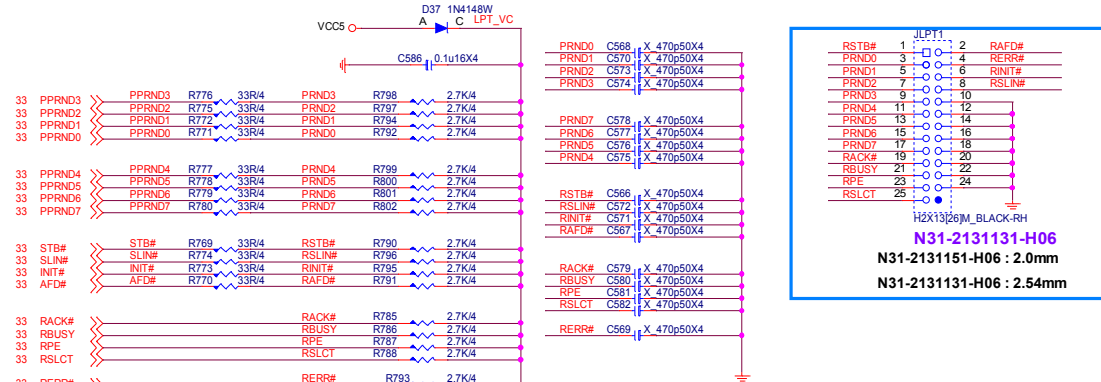


11/30 Modify to SILEGO Sequence

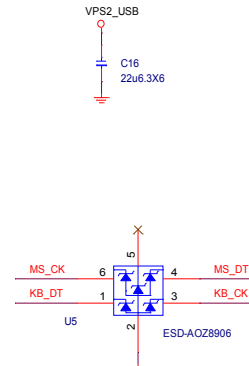
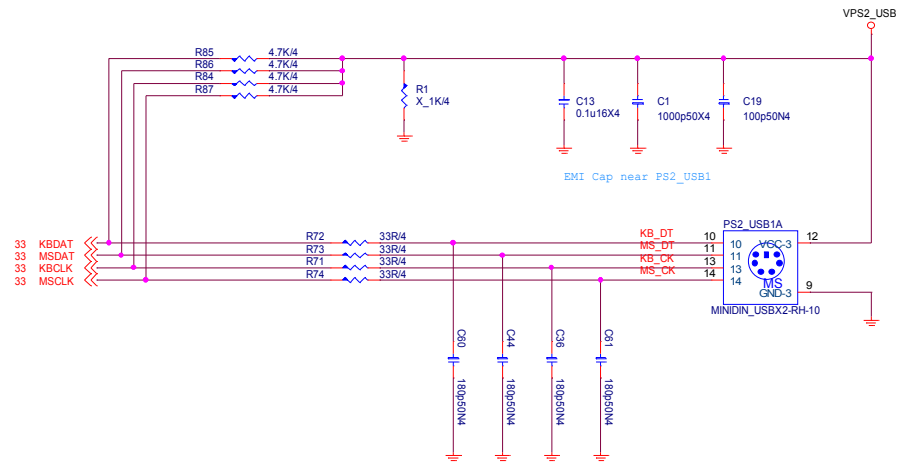
## SERIAL PORT 1



## PARALLAL PORT



### PS2 Connector

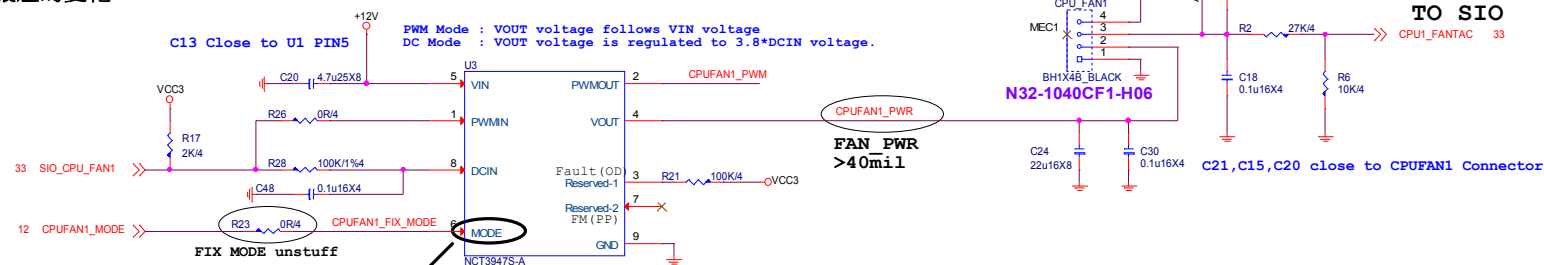


Main:D0G-05A0529-A68  
AVL:D0G-45B0510-I14

### NEAR CONNECTOR

```
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
```

1. PWM/DC/OCF LED (現在是改成R/G/B3色LED)
2. GPIO可以由BIOS切換 PWM/DC MODE
3. OCF拉回GPIO給BIOS認
4. PWM OR DC FAN拉回GPIO給BIOS認
5. FAN轉速加快的時候由SOFTWARE控制GPIO讓燈的變化

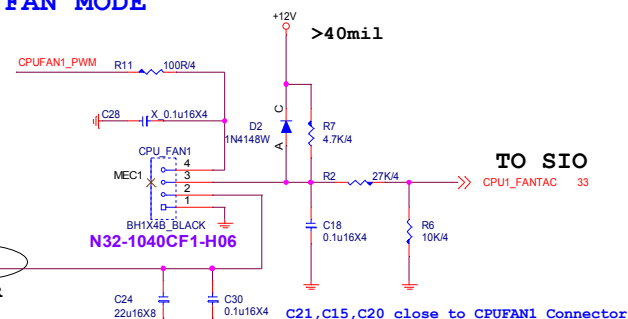


## GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V	
-------------------------	--



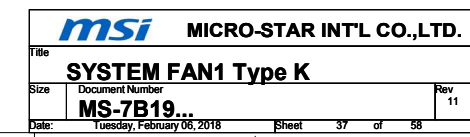
**Avoid NCT3947S MODE PIN Leakage**

The diagram shows the MODE pin (VCC3) connected to a pull-up resistor R18 (X\_10K/4) and a pull-down resistor R19 (X\_10K/4) to ground. A capacitor C41 (1u6) is connected to the MODE pin. The pin is labeled CPUFAN1\_FIX\_MODE.

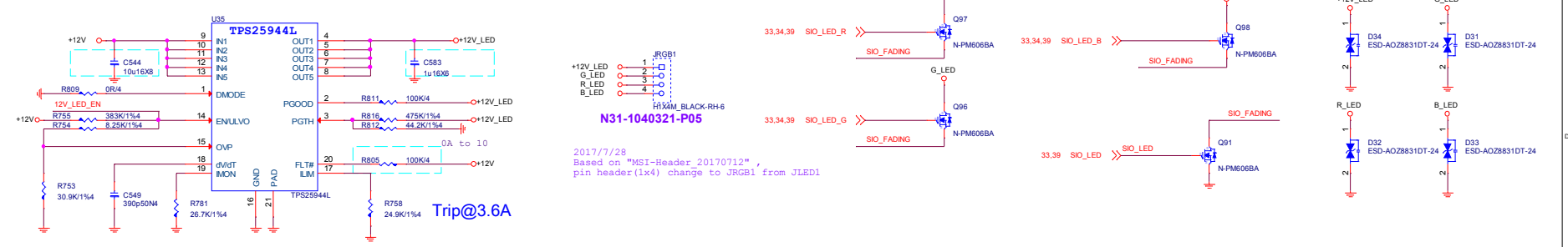
Resever For FIX DC or PWM MODE USE By PM SPEC



## 2.GPIO可以由BIOS切換 PWM/DC MODE



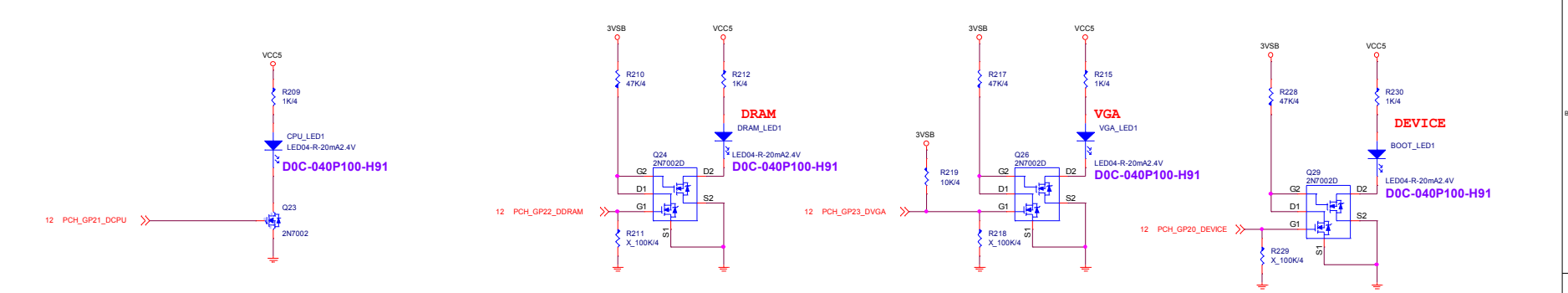
JLED



BOTTOM LED



EZ DEBUG

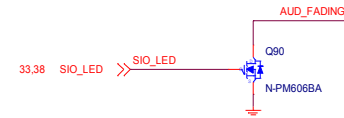
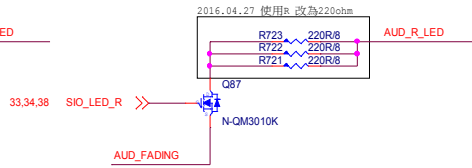
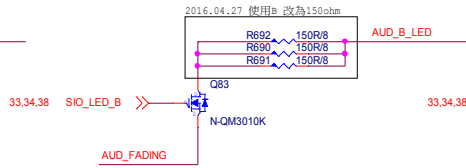
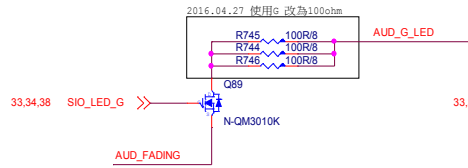
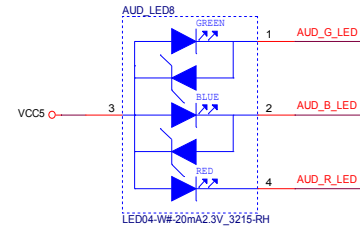
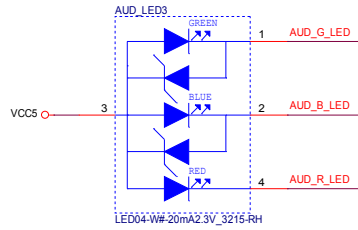
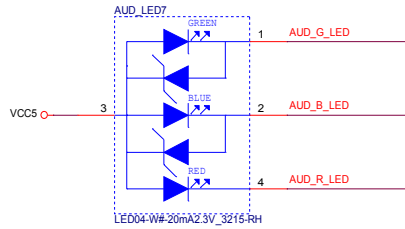
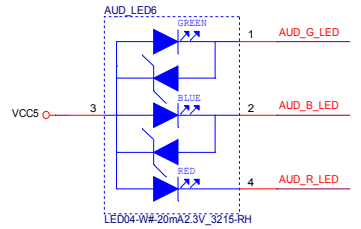
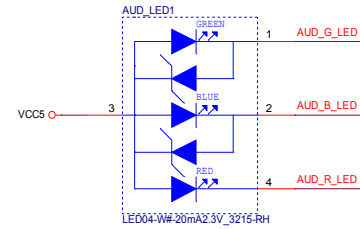
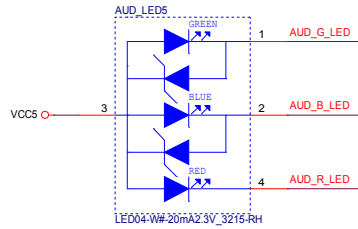
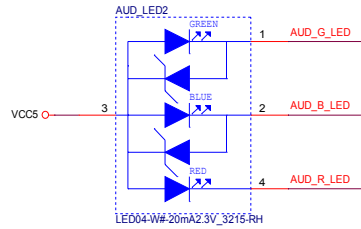
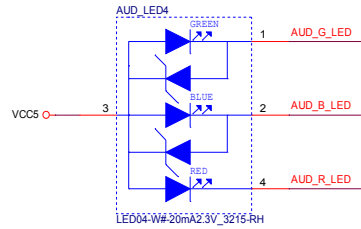


關機斷電狀態下，4個LED先維持default全暗，開機通電後：  
1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。  
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。  
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。  
4. 因此最後正常順利開機後，三個LED燈都是減掉的。  
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

GPIO LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
減	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

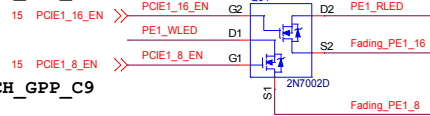
## AUDIO\_LED

Audio moat is transparent and width 40mil

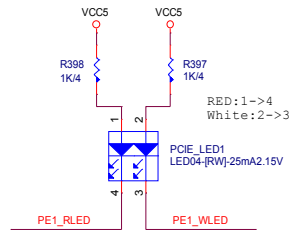
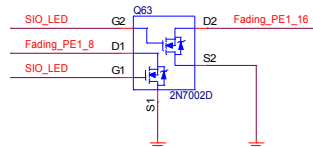


## PCIE1\_LED

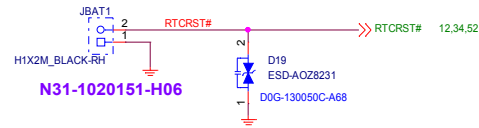
### PCH\_GPP\_C8



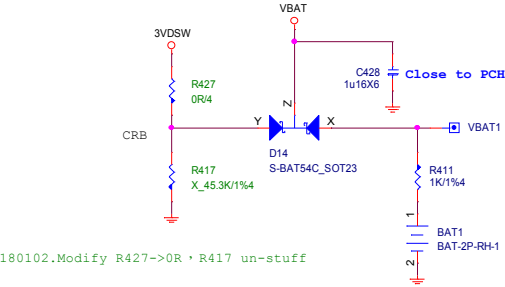
### PCH\_GPP\_C9



CUT VBAT

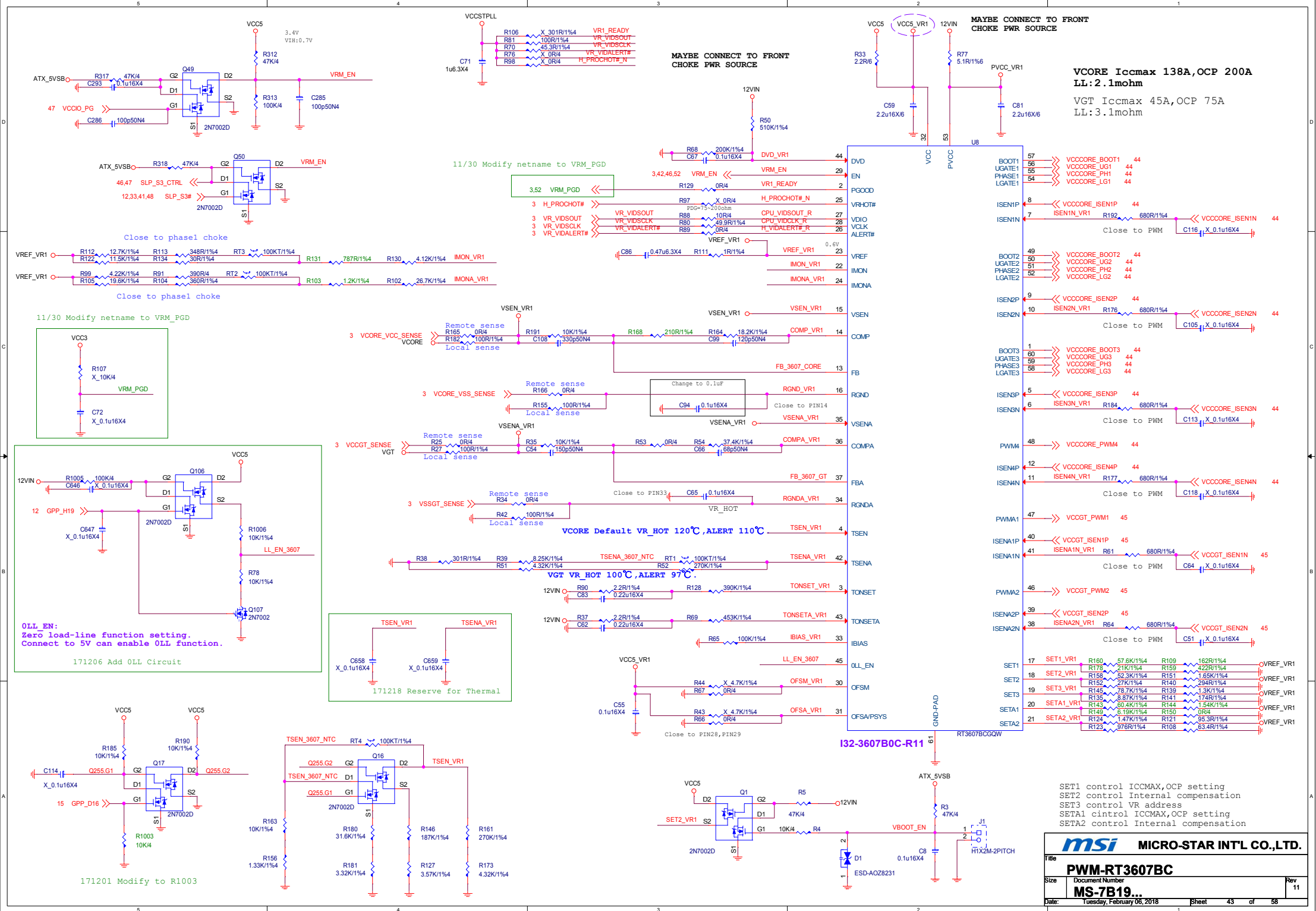


VBAT



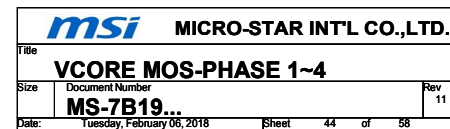
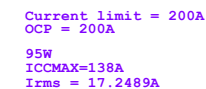






D03-4337N0C-ST8: 7.1 mohm

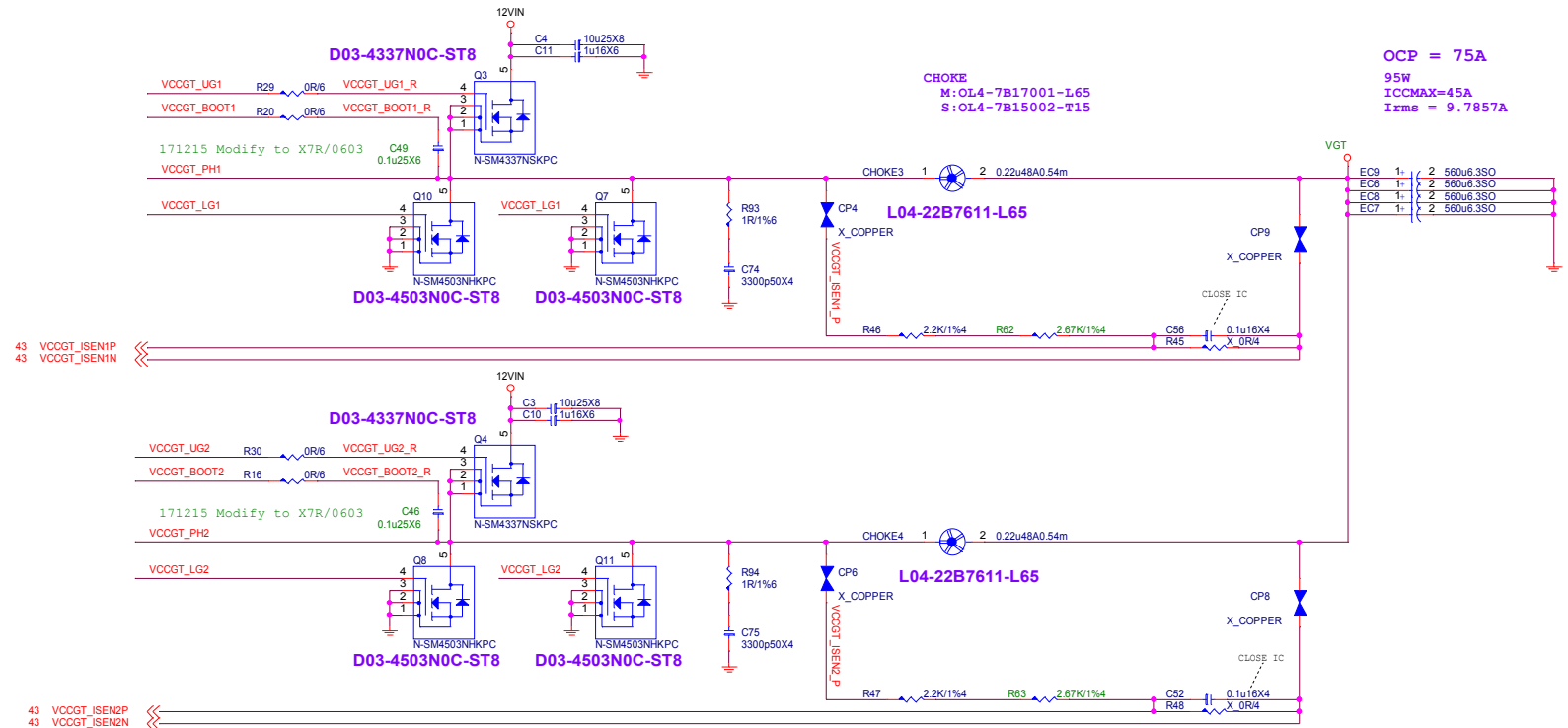
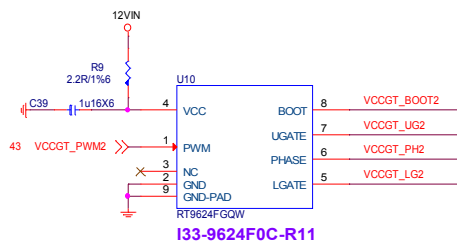
D03-4503N0C-ST8: 3 mohm





D03-4337N0C-ST8: 7.1 mohm

D03-4503N0C-ST8: 3 mohm



ATX\_5VSB

R373  
47K/4

C340  
X 0.1u16X4

3.42,43.52 VRM\_EN

R370  
0R/4

47 VCCIO\_EN

R369  
X 0R/4

Q55  
2N7002D

G2  
D2  
G1  
S2

VCCSA\_EN

C645  
0.1u16X4

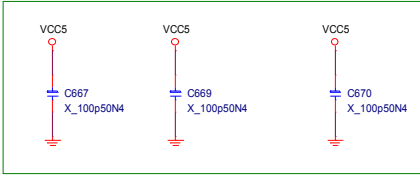
VCCSA\_EN

43.47 SLP\_S3\_CTRL

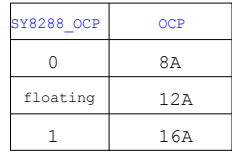
Q57  
2N7002

**SLP\_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.**

SLP\_S3# assertion to VR disabled  
max:lus



IMAX 10A  
ILIMIT=10A~12A  
IOC=ILIMIT+40%\*IMAX/2=12A~14A.

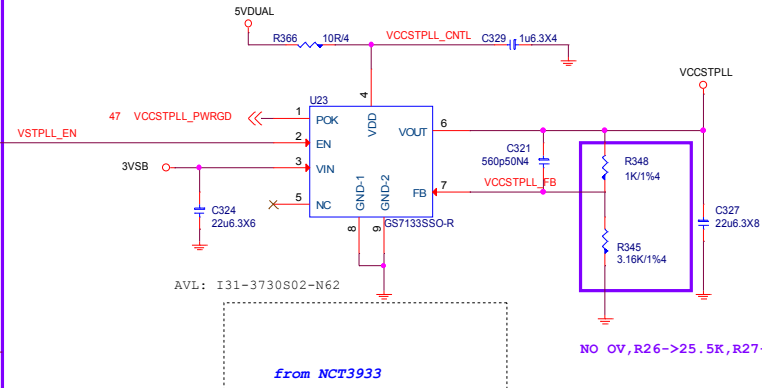
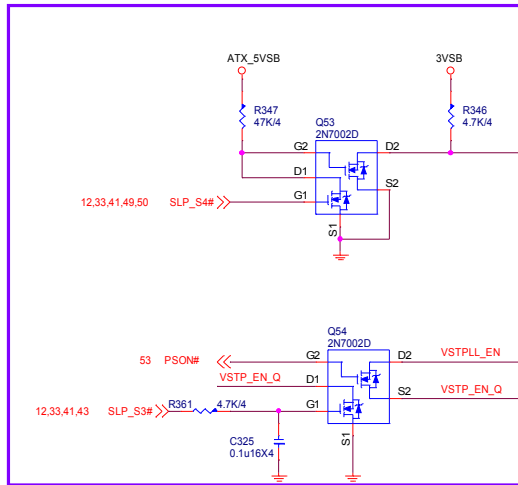


# VCCSTPLL

1.05V; 230mA

For Cost down VCCST&VCCPLL merge

VCCST:80mA  
VCCPLL:150mA



NO OV,R26->25.5K,R27->100K, C178 unstuff

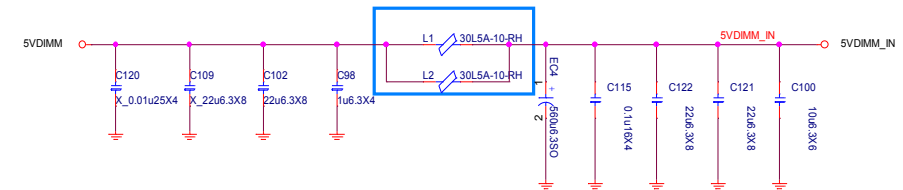
VCCIO ramped and stable before  
beginning of VCCOPC/VCCEPIO ramp

VCCST/PLL stable 1ms before PROC\_PWRGD

DDR4\_1.2V 3.3A+ 7.85A+0.375A=11.525A

3.3A FOR CPU  
7.85A FOR 2DIMM DDR4  
0.375A FOR VTT\_DDR

$I_{in} = 9.525A \times 1.2V / 0.8 / 5V = 2.8575A$   
L02-3008043-M26  
Over 85°C, Rated Current 1.5A.



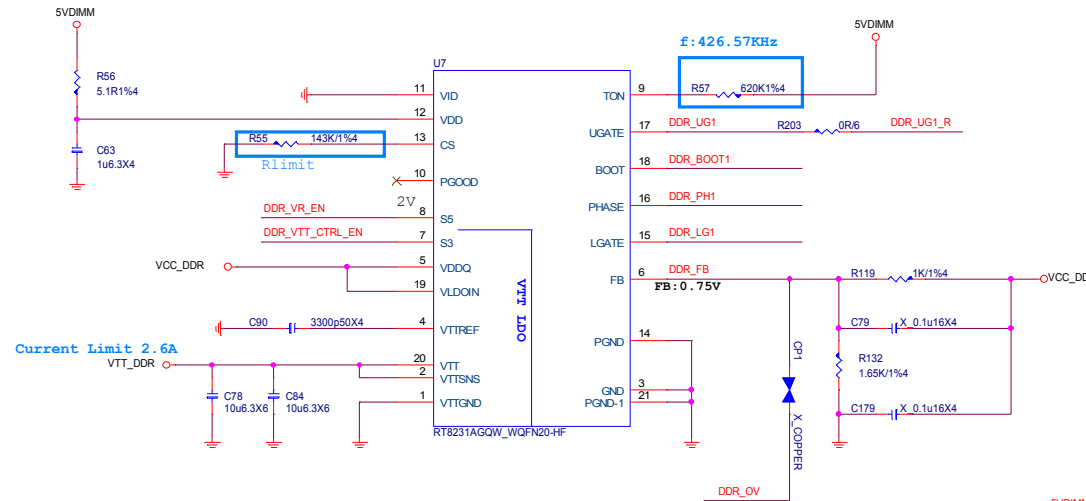
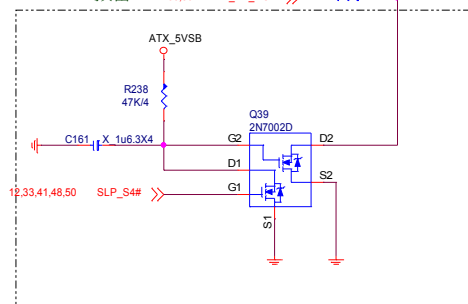
VID	Reference Voltage (V)
H	0.675
L	0.75

$$I_{rms} = I_{out} \times \sqrt{((V_{out}/V_{in}) \times (1 - (V_{out}/V_{in})))}$$
$$= 9.525 \times 0.427$$
$$= 4.06797A$$

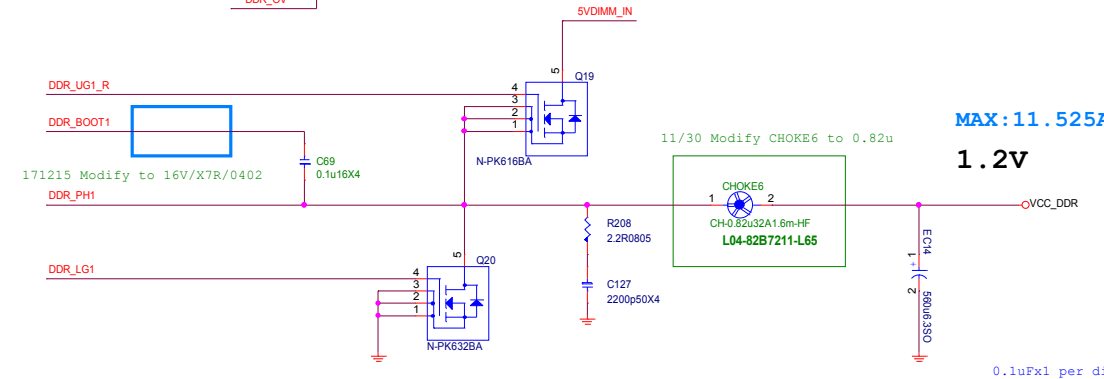
171219 Modify to VPP\_VR\_PG Control

From SIO pin 87

33 SIO\_VDDQ\_EN >> R247 0R/4  
33.50 VPP\_VR\_PG >> R250 0R/4

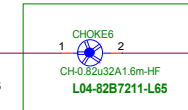


Current Limit 2.6A  
VTT\_DDR

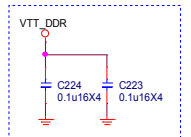


MAX: 11.525A  
1.2V

11/30 Modify CH0KE6 to 0.82u

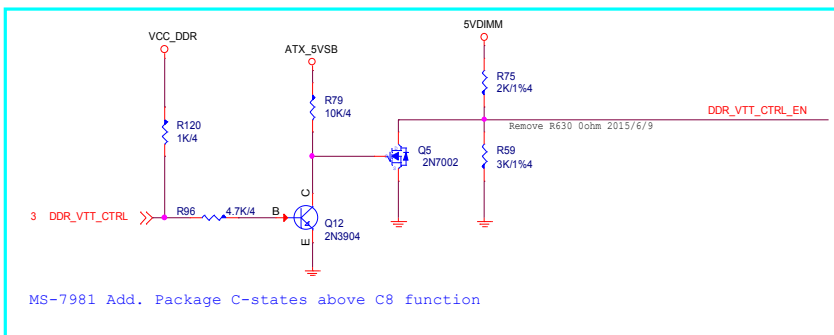


0.1uFx1 per dimm



SLP\_S4# de-assertion to VDDQ ramp down start

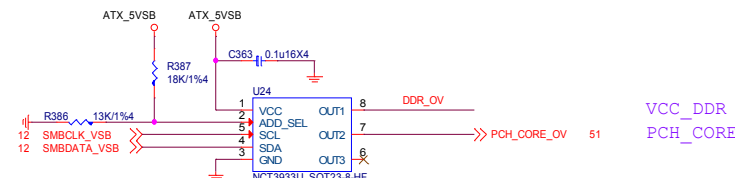
VPP ramp down after VDDQ ramp down



MS-7981 Add. Package C-states above C8 function

### UPI VOLTAGE CONSOLE

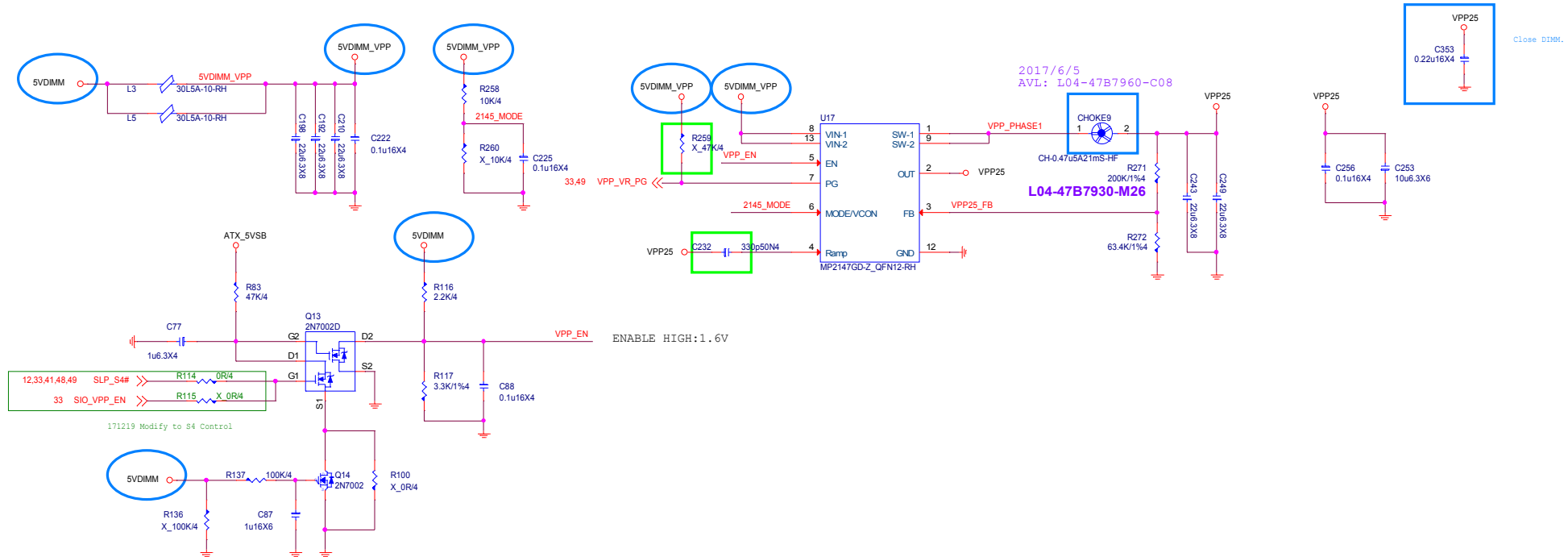
0x26: RH=18K, RL=13K



VCC\_DDR  
PCH\_CORE

4DIMM :2.24A FOR  
DDR VPP2.5V

**VPP25 Power**  
**2.5V; 2.24A**



To make sure VPP EN after 5VDIMM stable

# PCH 1P05\_VSB

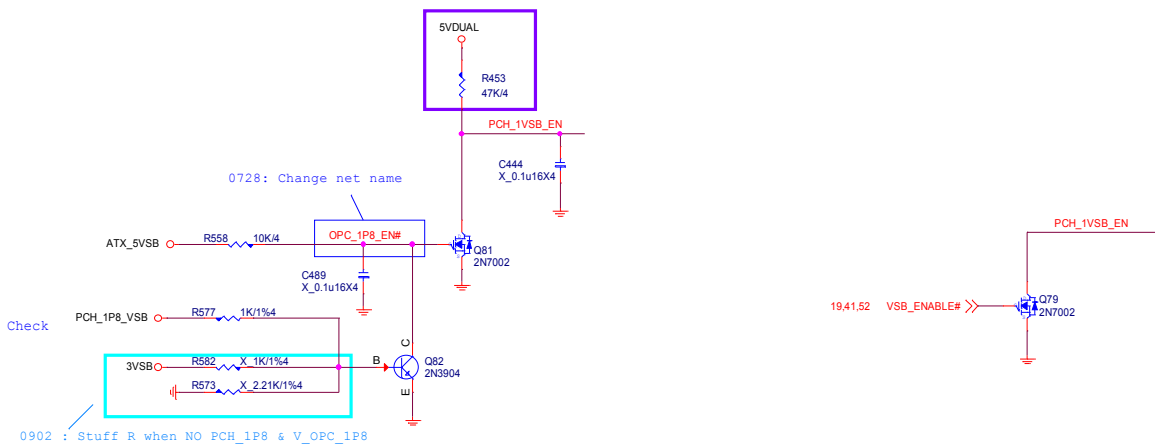
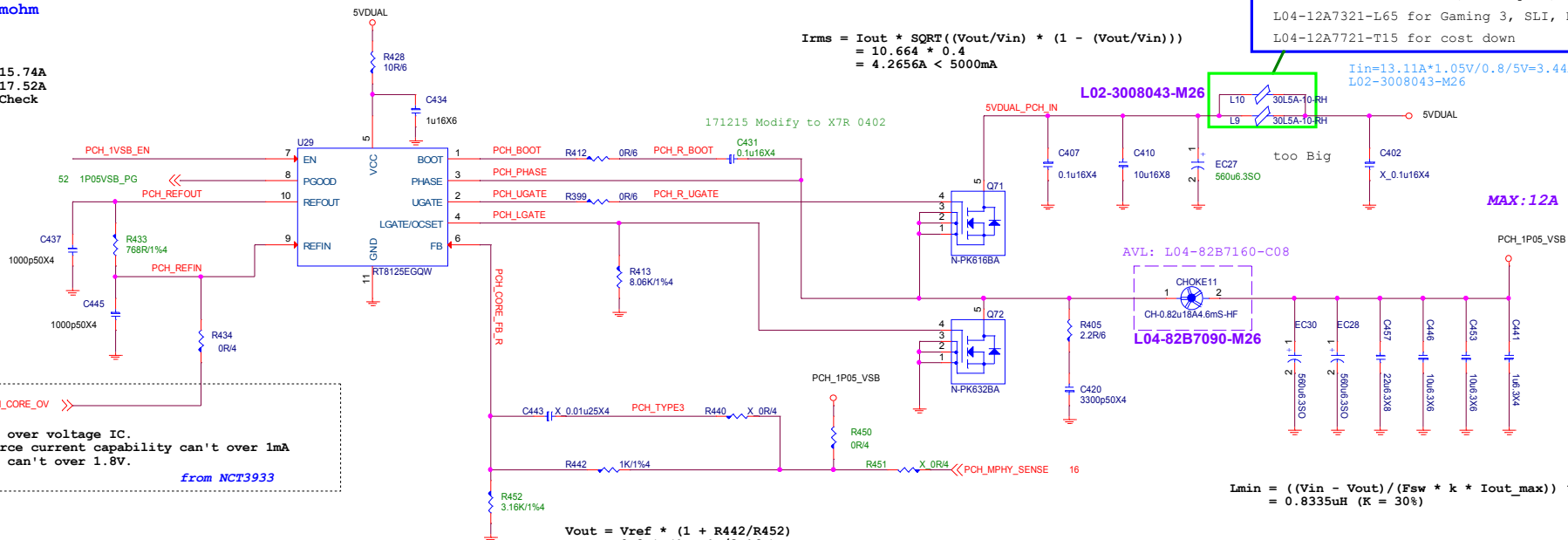
1.05V; 12A

Rocpset:3.48K  
OCP=Rocset\*10uA/Rdson(Low side)  
=8.06K\*10uA/5.1mohm  
=15.8A

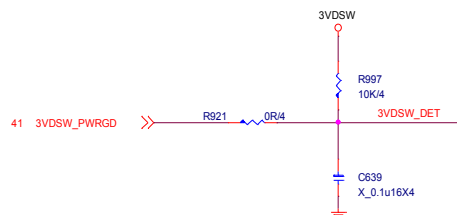
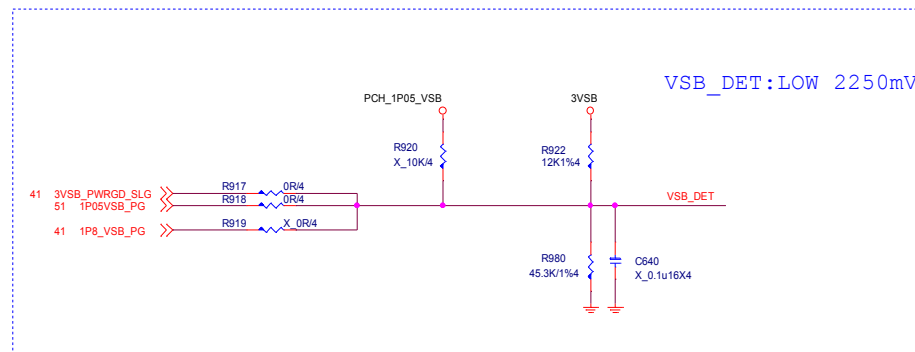
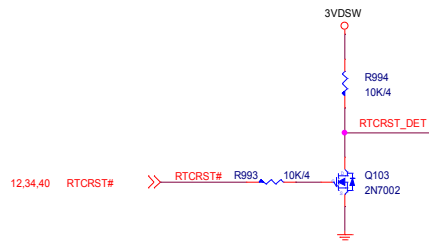
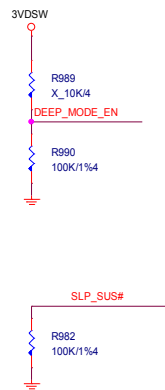
Rocs:8.06K,OCP:  
D03-4C05N03-O05 : 15.74A  
D03-632BA0C-N03 : 17.52A  
use UBIQ MOS need Check

Rdson (low) 4.5V

D03-3116M00-U47 : 3.6 mohm  
D03-632BA0C-N03 : 4.6mohm  
D03-3056M00-U47 : 6.2mohm

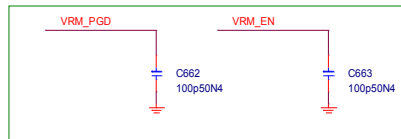
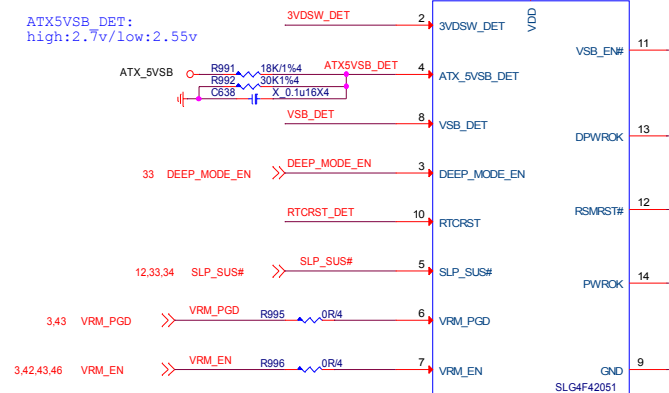


	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0

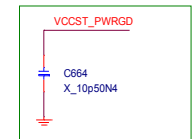
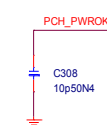


19 ATX5VSB\_DET

ATX5VSB\_DET:  
high:2.7v/low:2.55v



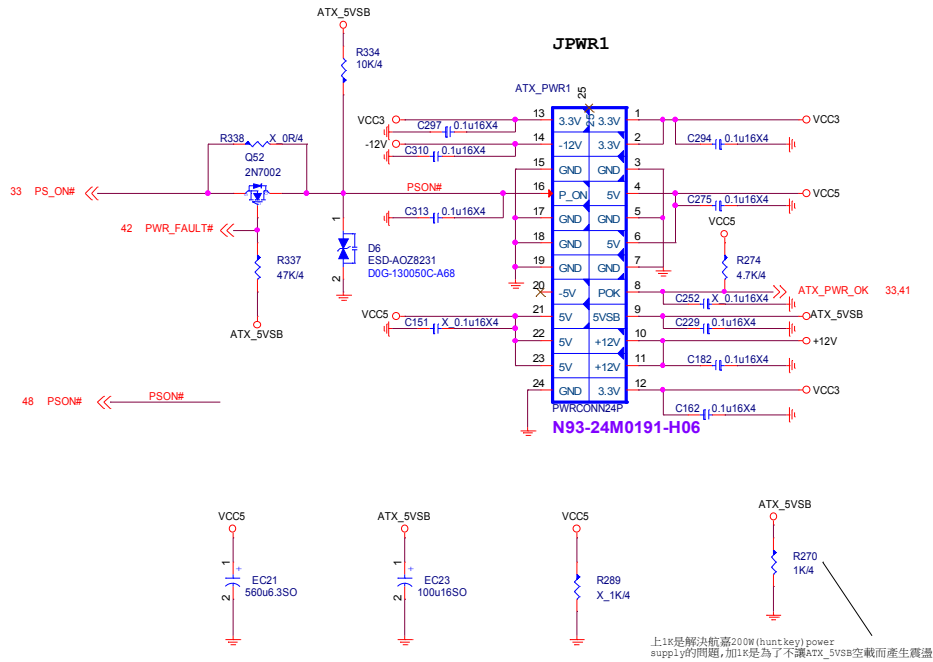
180201:Add C662 C663



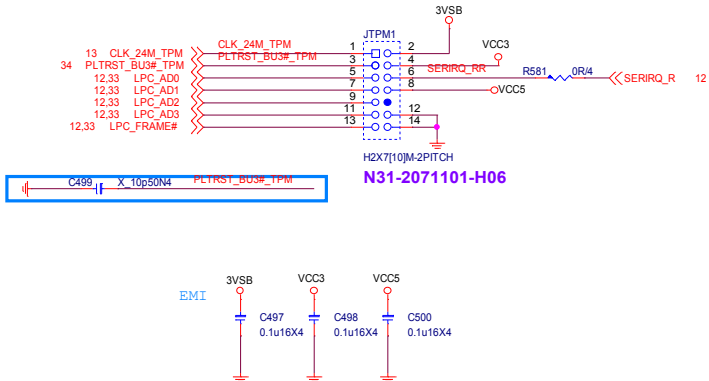
180201:Add C664



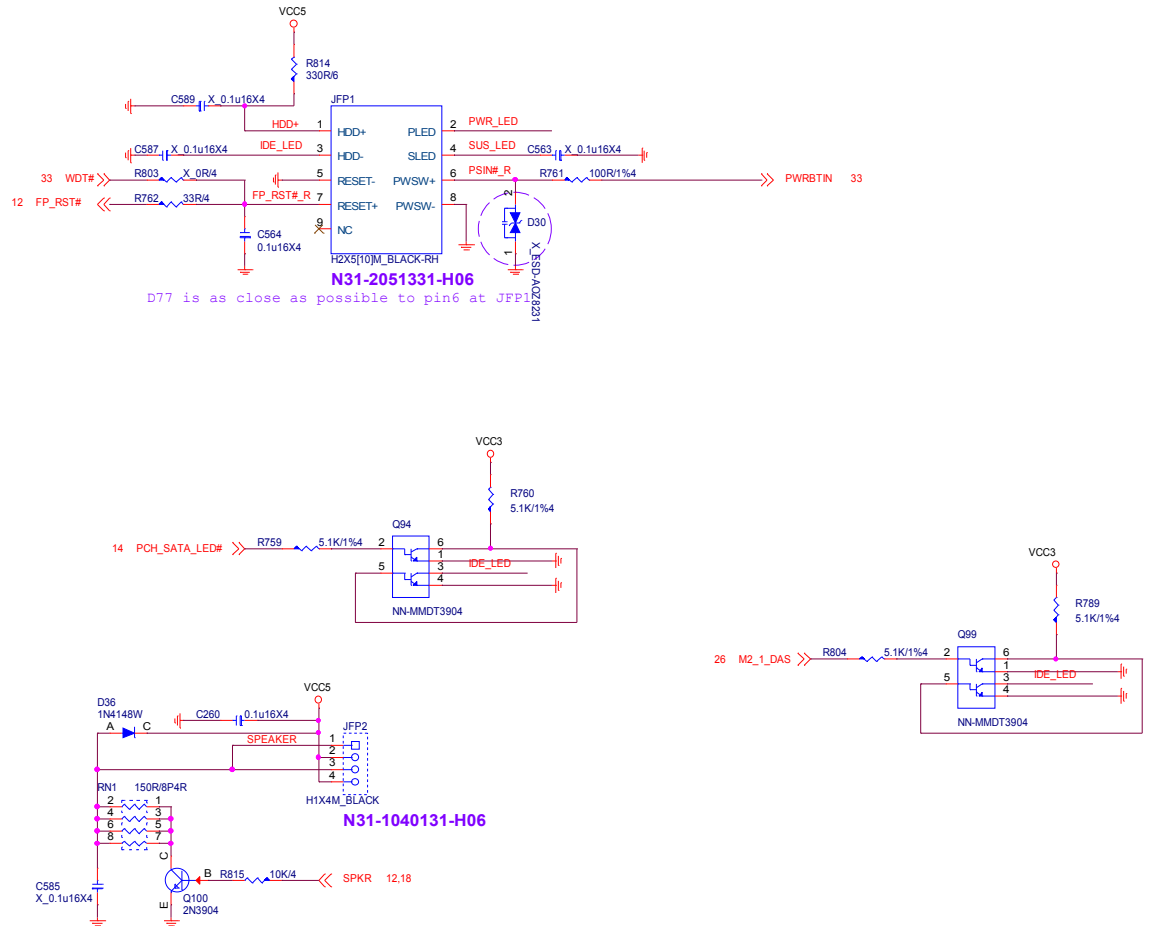
## ATX POWER CONNECTOR



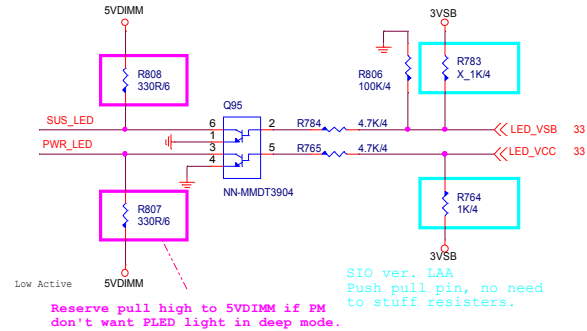
## TPM Pin Header



## FRONT PANEL



## Front Panel LED





PD0-07B1911-G37, 精成-深圳, 22, 寶安恩斯邁廠 (MSIS)  
PD0-07B1911-E48, 競華, 22, 寶安恩斯邁廠 (MSIS)



G51-M1SPXXA-A09



Y01-RHDMI03-000



Y02-MU00170-CFO



Y02-MA00101-SSE



Y02-MA00401-XSP



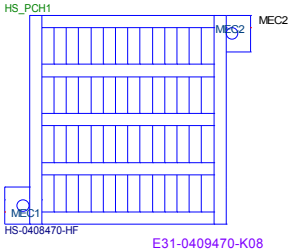
E21-7869020-F02



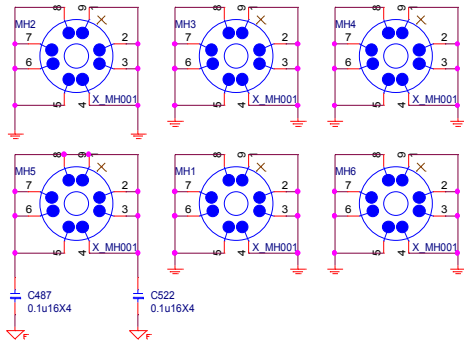
D06-0100101-P01



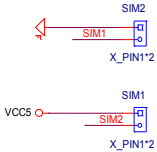
Y02-MU00100-NAH



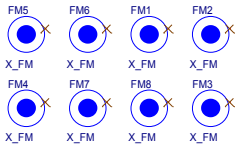
## Mounting Holes



## Simulation



## Optical Fiducial Marks-120



## Vcheck

PCH_1P05_VSB		PCH_1P05_VSB	VCORE		VCORE
VCCSTPLL		VCCSTPLL	VGT		VGT
VPP25		VPP25	VCC_DDR		VCC_DDR
1P8_VSB		1P8_VSB	VCCSA		VCCSA
3VSB		3VSB	VCCIO		VCCIO
3VDSW		3VDSW	VTT_DDR		VTT_DDR